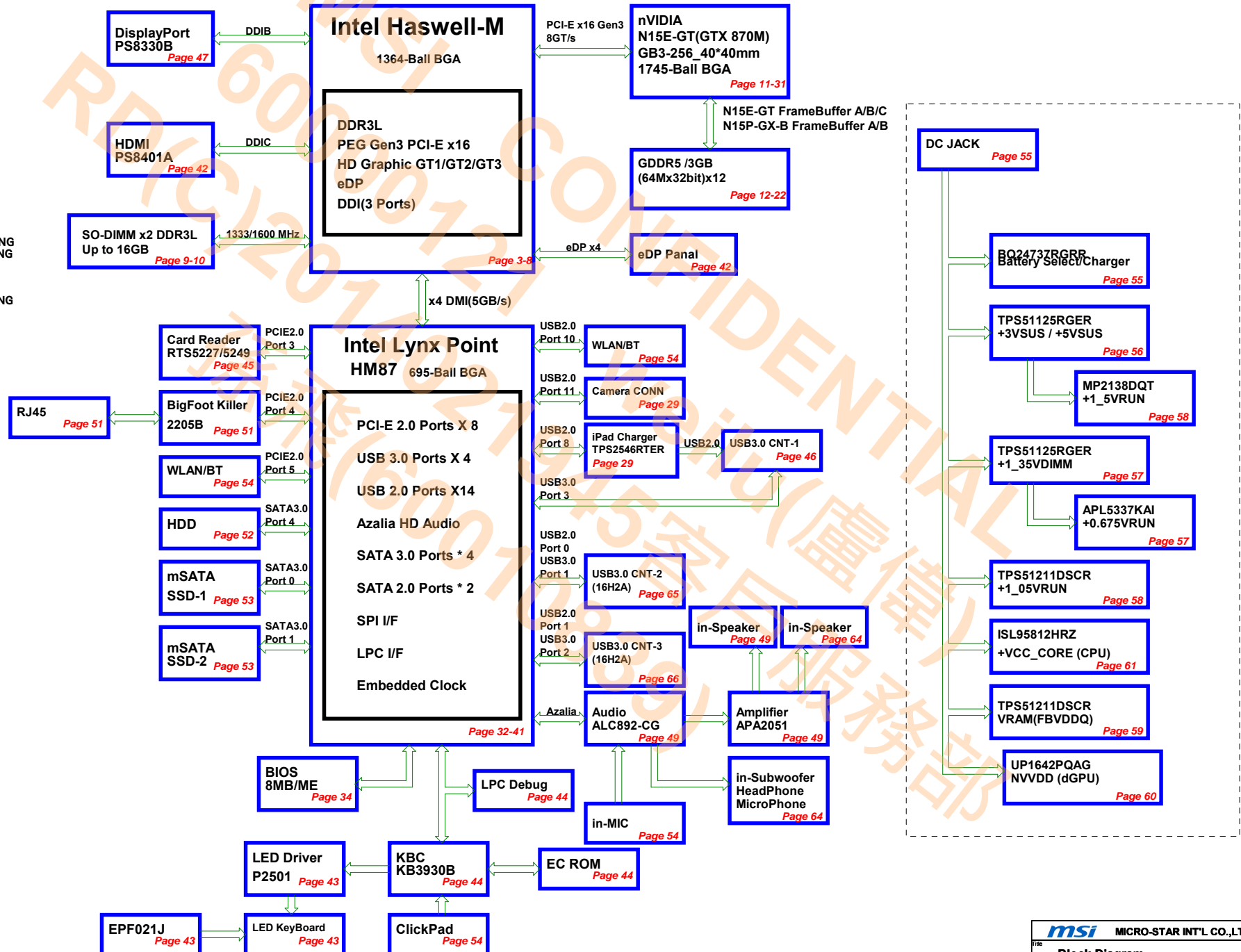


Page 01:	Block Diagram
Page 02:	Platform
Page 03:	CPU-1 (Host Bus)
Page 04:	CPU-2 (DDR3L)
Page 05:	CPU-3 (Display/Reserved)
Page 06:	CPU-4 (Power)
Page 07:	CPU-6 (Power & GND)
Page 08:	CPU-5 (GND)
Page 09:	DDR3L SODIMM 0
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Page 11:	DGPU PCI-E Host
Page 12:	DGPU_MEM IF A/B
Page 13:	DGPU_GDDR5 FrameBuffer A0
Page 14:	DGPU_GDDR5 FrameBuffer A1
Page 15:	DGPU_GDDR5 FrameBuffer B0
Page 16:	DGPU_GDDR5 FrameBuffer B1
Page 17:	DGPU_GDDR5 FB-A_DECOUPLING
Page 18:	DGPU_GDDR5 FB-B_DECOUPLING
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Page 21:	DGPU_GDDR5 FrameBuffer C
Page 22:	DGPU_GDDR5 FB-C_DECOUPLING
Page 23:	DGPU_GPU DECOUPLING A
Page 24:	DGPU_GPU DECOUPLING B
Page 25:	DGPU_DACA_Display IF
Page 26:	DGPU_GPIO_I2C
Page 27:	DGPU_MIO & XTAL
Page 28:	DGPU_ROM_HW Straps
Page 29:	DGPU_NVVDD, FBVDDQ
Page 30:	DGPU_GND
Page 31:	DGPU_Power Control
Page 32:	PCH-1 (HDA/JTAG/SATA)
Page 33:	PCH-2 (CLK)
Page 34:	PCH-3 (LPC, SMBUS)
Page 35:	PCH-4 (DMI, FDI)
Page 36:	PCH-5 (PCI, DDI)
Page 37:	PCH-6 (GPIO, MISC)
Page 38:	PCH-7 (PCI, USB)
Page 39:	PCH-8 (Power)
Page 40:	PCH-8 (Power)
Page 41:	PCH-8 (GND)
Page 42:	eDP Connector
Page 43:	LED Driver IC/LED_8051
Page 44:	KBC (KB3930QFB1)
Page 45:	Card Reader/USB3.0 CNT-1/-2
Page 46:	USB 3.0 / iCharger
Page 47:	DP with Repeater
Page 48:	HDMI Repeater
Page 49:	Audio CODEC/Audio AMP
Page 50:	CPU FAN/BTB CONN
Page 51:	GIGA LAN(BigFoot BFN2205B)
Page 52:	HDD With Repeater
Page 53:	SSD / DGPU FAN
Page 54:	WLAN / Camera/ClickPad/LID
Page 55:	Battery Select/Charger
Page 56:	System Power
Page 57:	+1.35VDIMM/+0.675VRUN
Page 58:	+1.05VRUN / +1.5VRUN
Page 59:	DGPU POWER FBVDDQ
Page 60:	DGPU POWER NVVDD
Page 61:	CPU Power (ISL95812HRZ)
Page 62:	EMI
Page 63:	Screw/ME
Page 64:	[A] Audio
Page 65:	[A] USB3.0 CNT-3/-4
Page 66:	LED Board
Page 67:	Power SW Board
Page 68:	Power Delivery Map
Page 69:	Power on Block Diagram
Page 70:	Power down Sequence
Page 71:	Power on Sequence



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

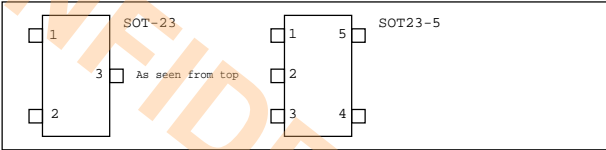
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVDD	V Core Voltage for nVIDIA dGPU	NVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVDD_EN

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAXxx = Like Test Point, but using VIA.

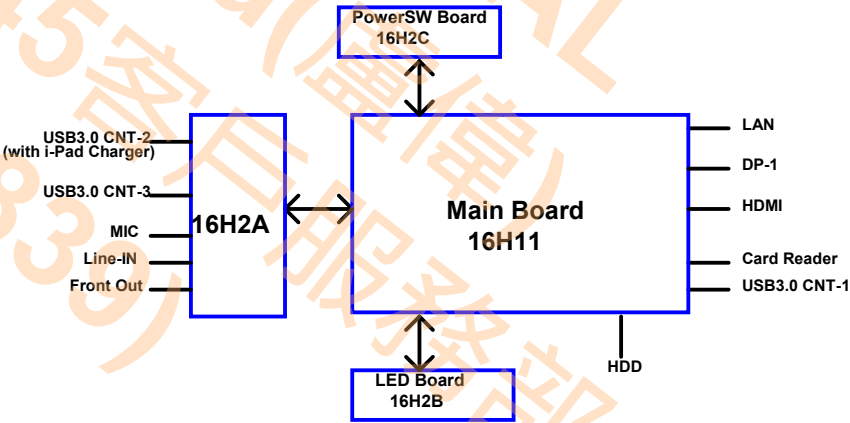
PCB Footprints



POWER STATES

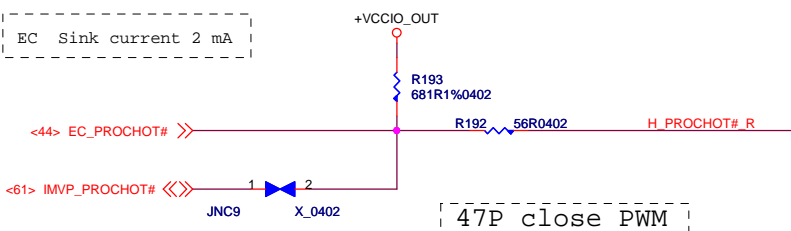
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high



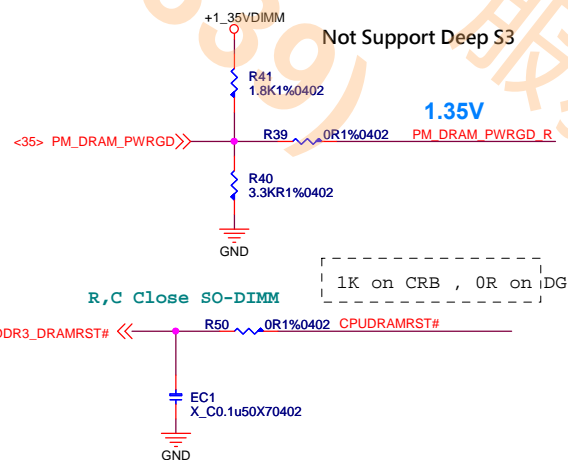
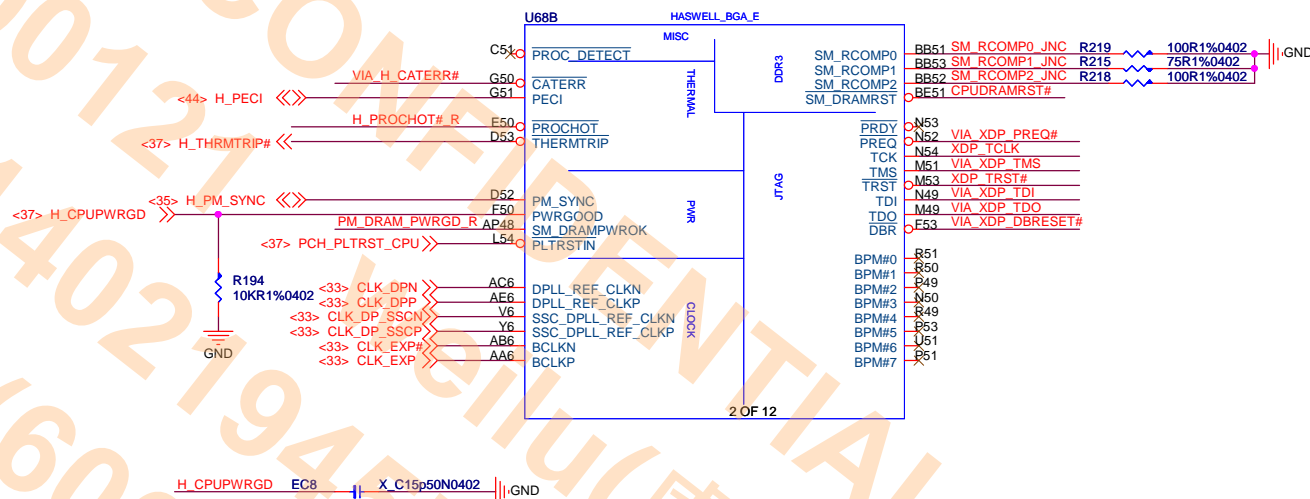
Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

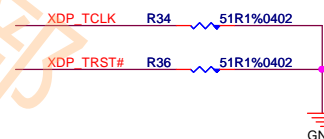


Haswell (CLK,MISC,JTAG)

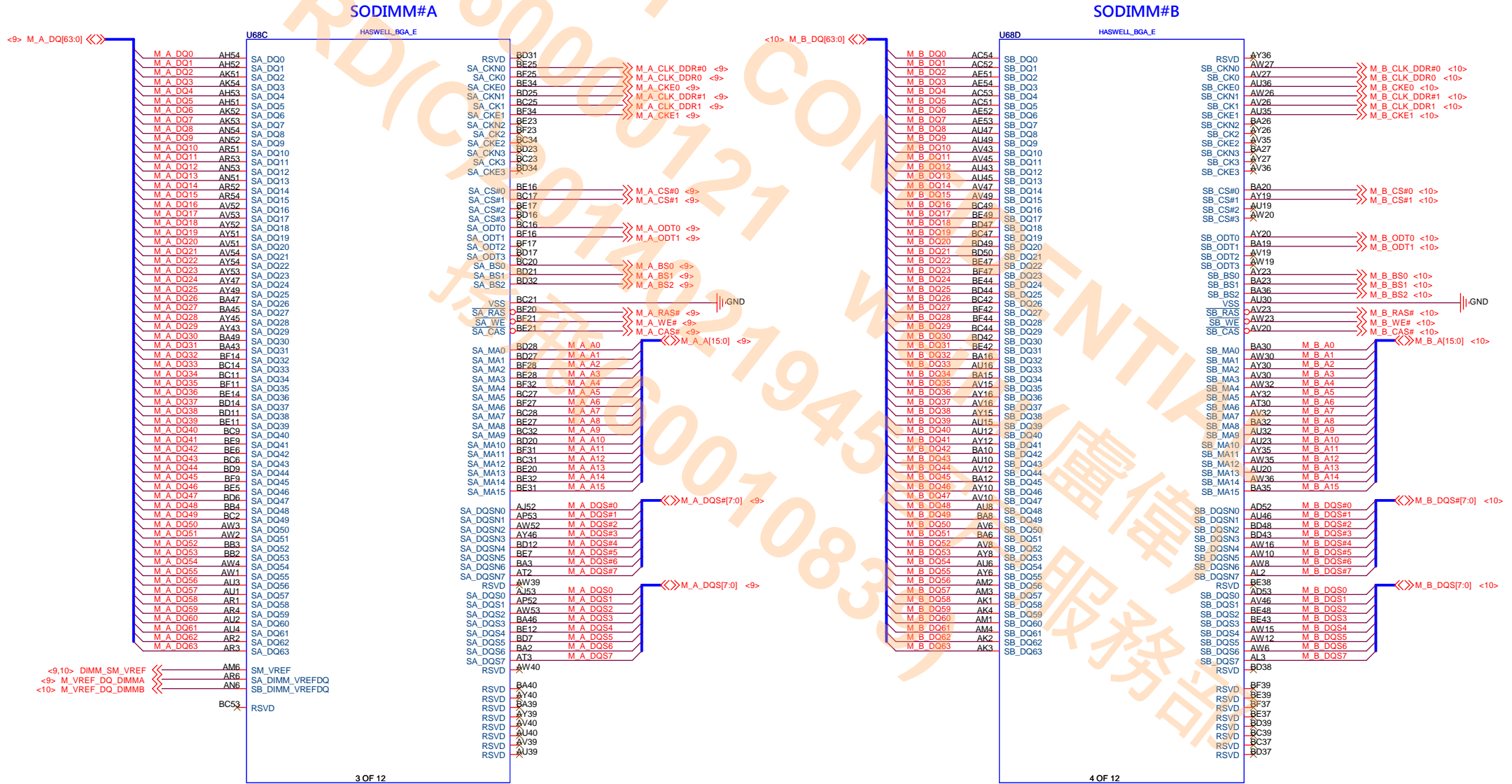
SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



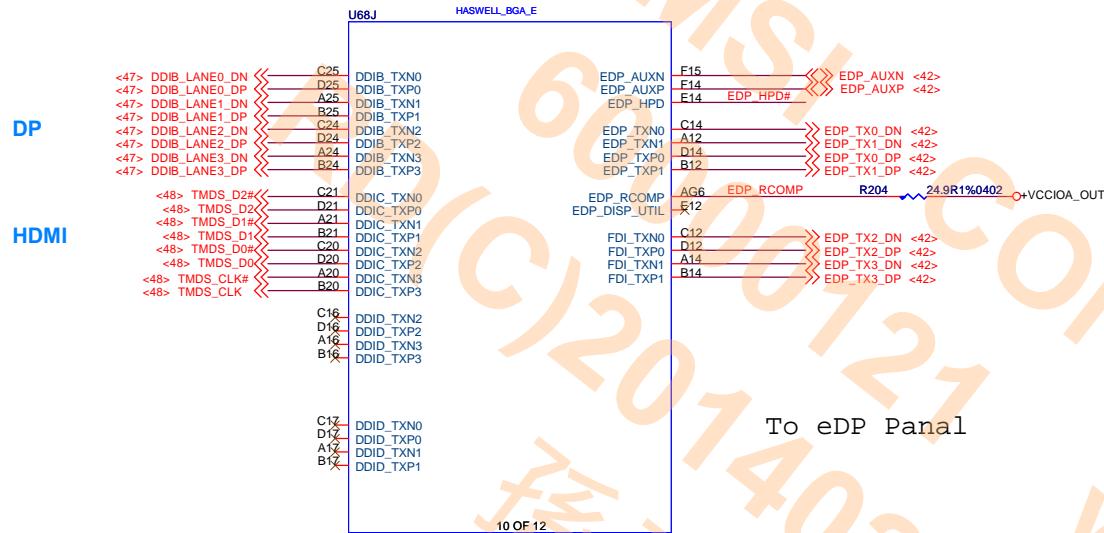
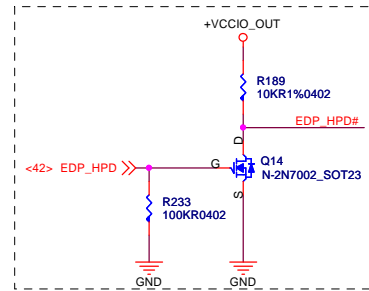
p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals,
PREQ# and PRDY# signals signals have adequate
internal bias resistances to support the removal of the
external pull up and pull down on the board
when debug is no longer needed.



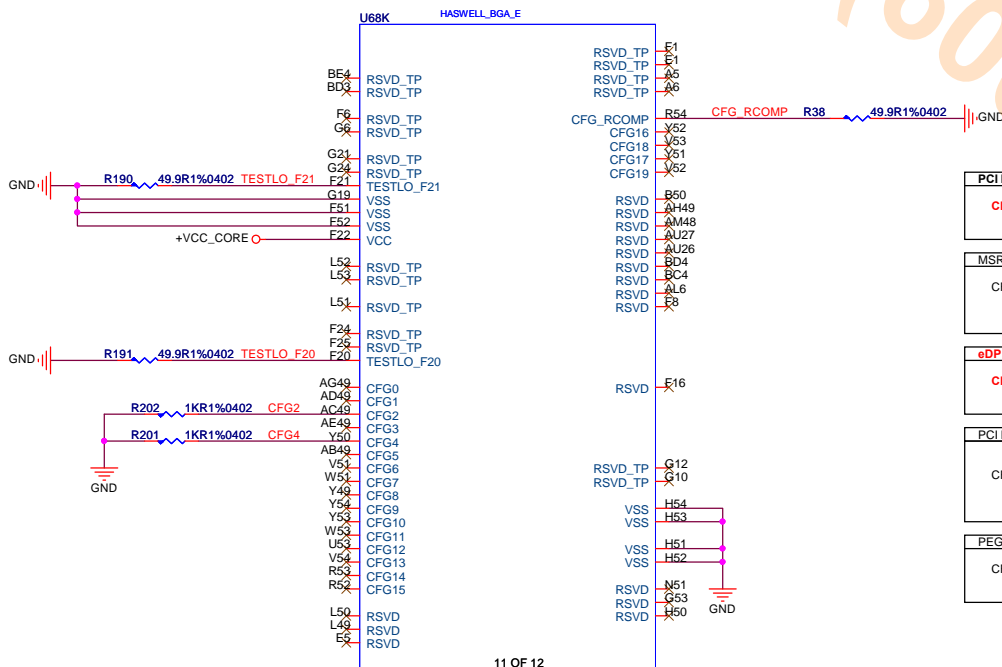
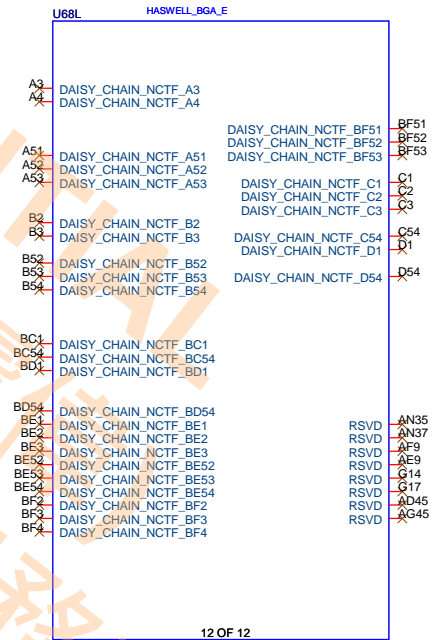
Haswell (DDR3L)



Display/Reserved



To eDP Panel



PCI Express® Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

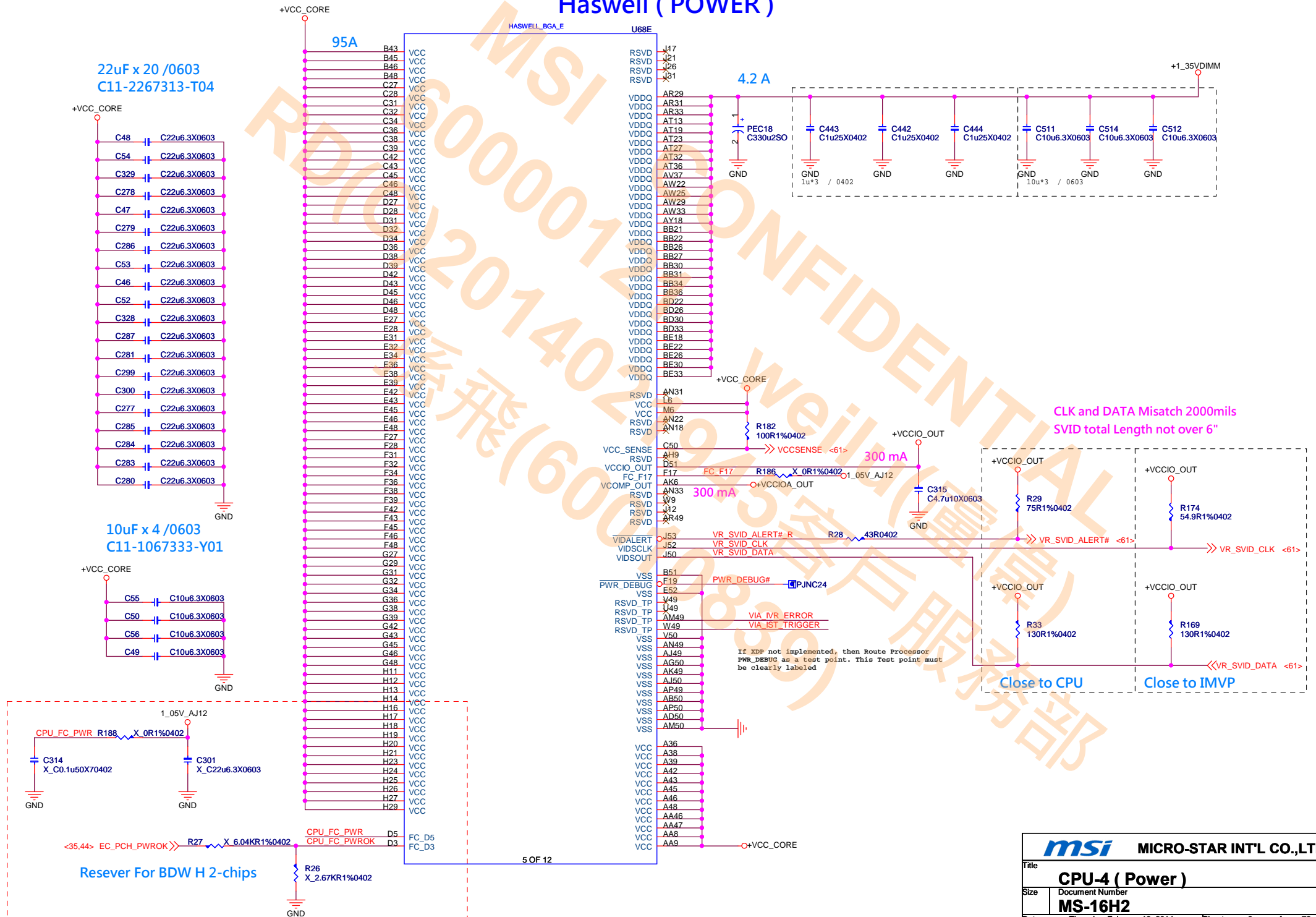
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

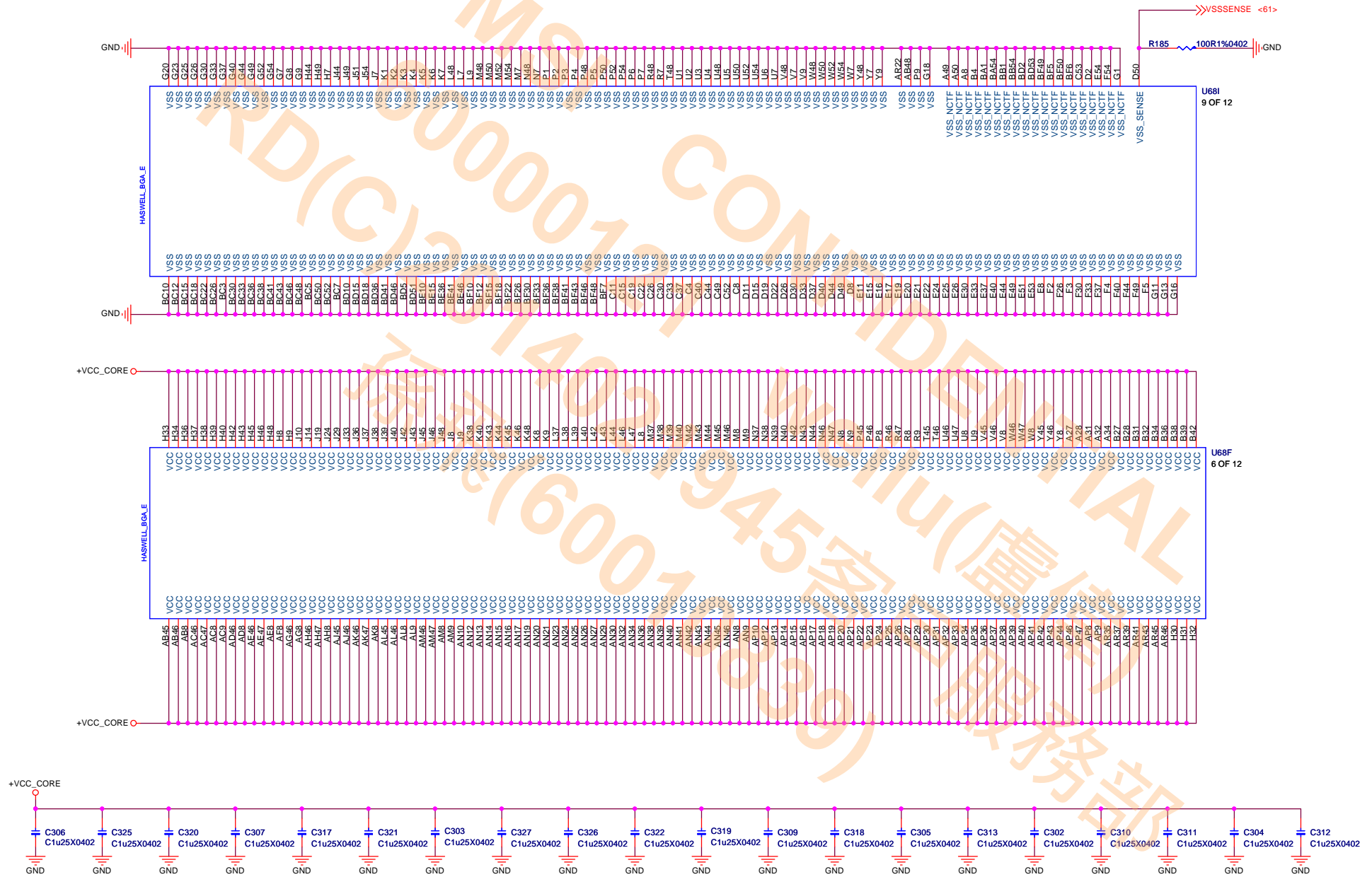
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

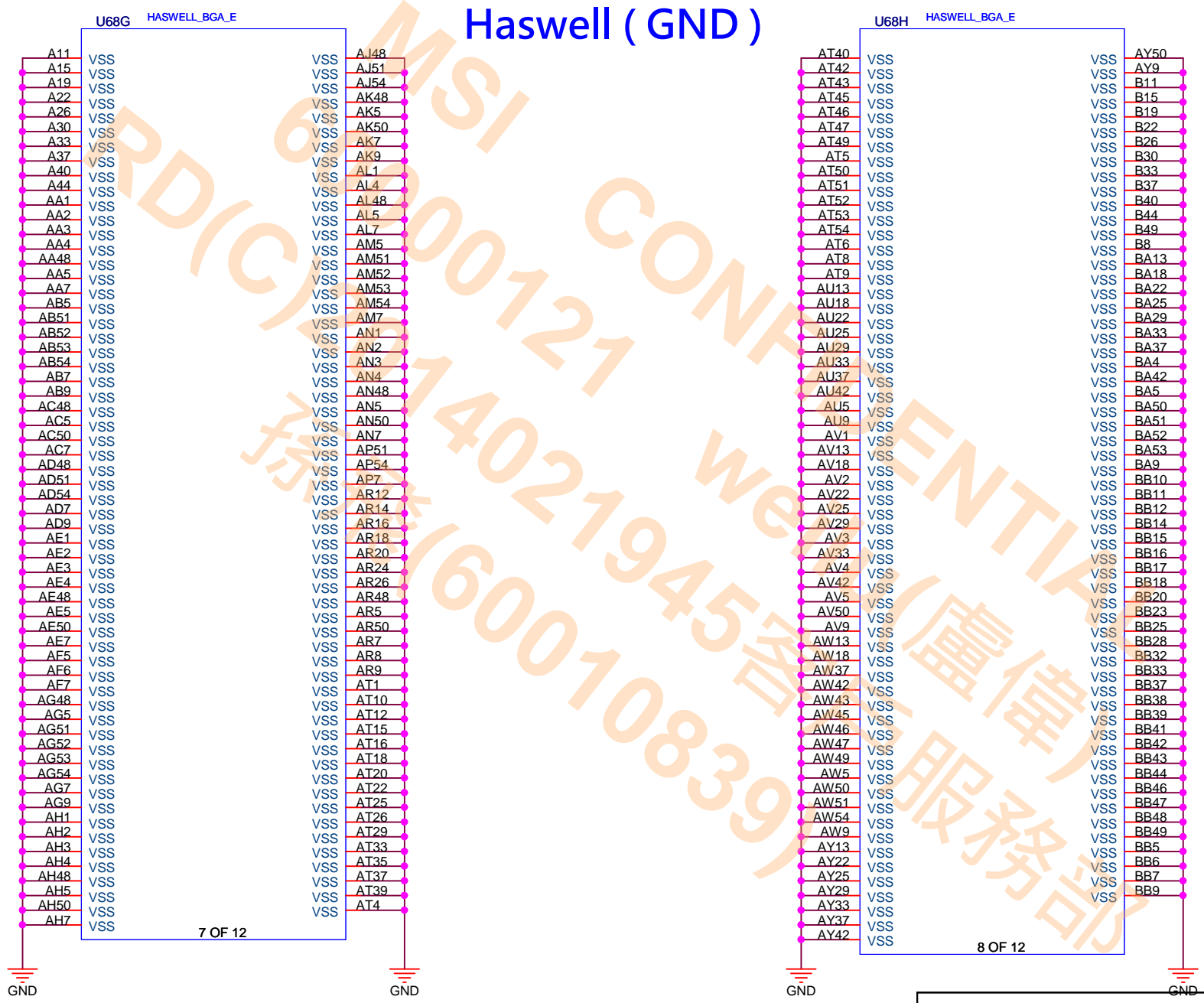
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Haswell (POWER)



Haswell (Power & GND)

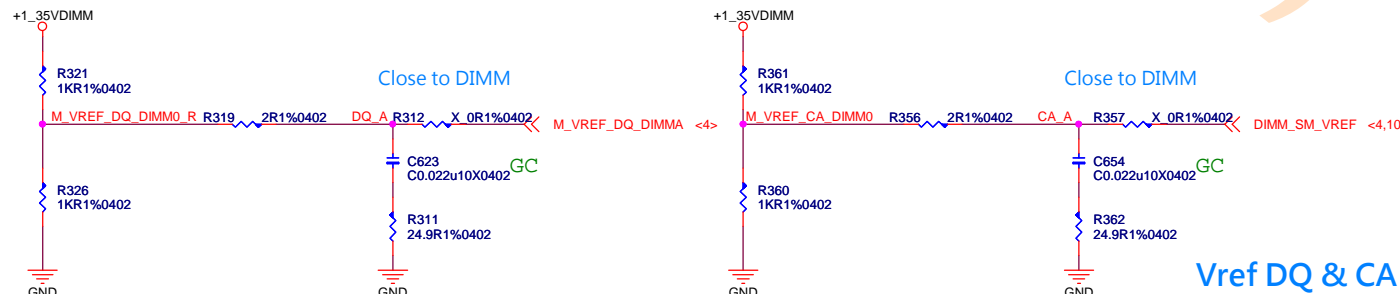
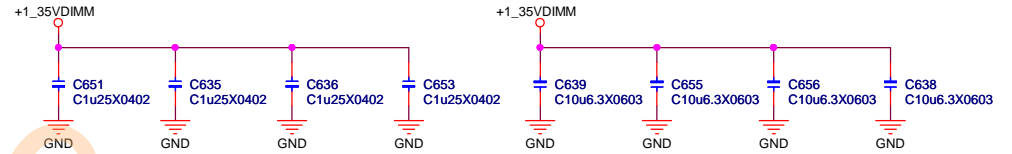




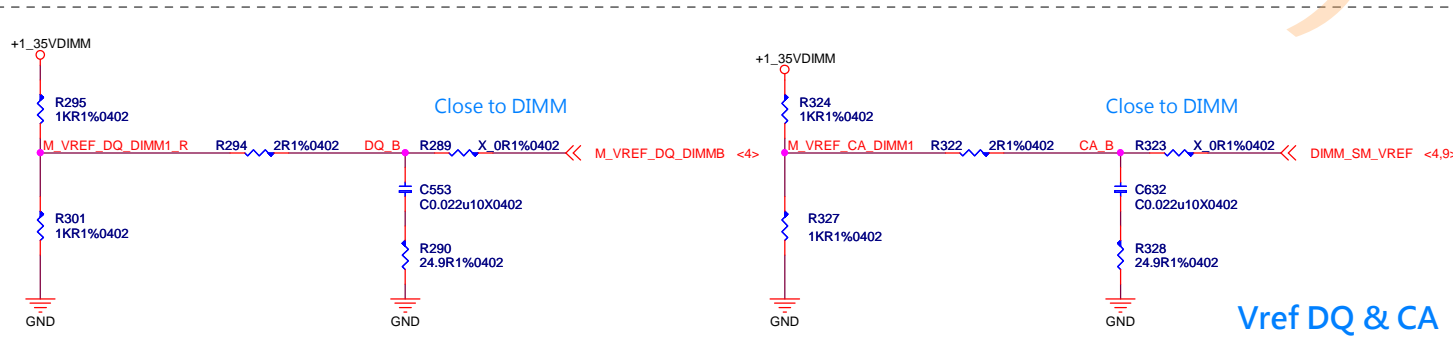
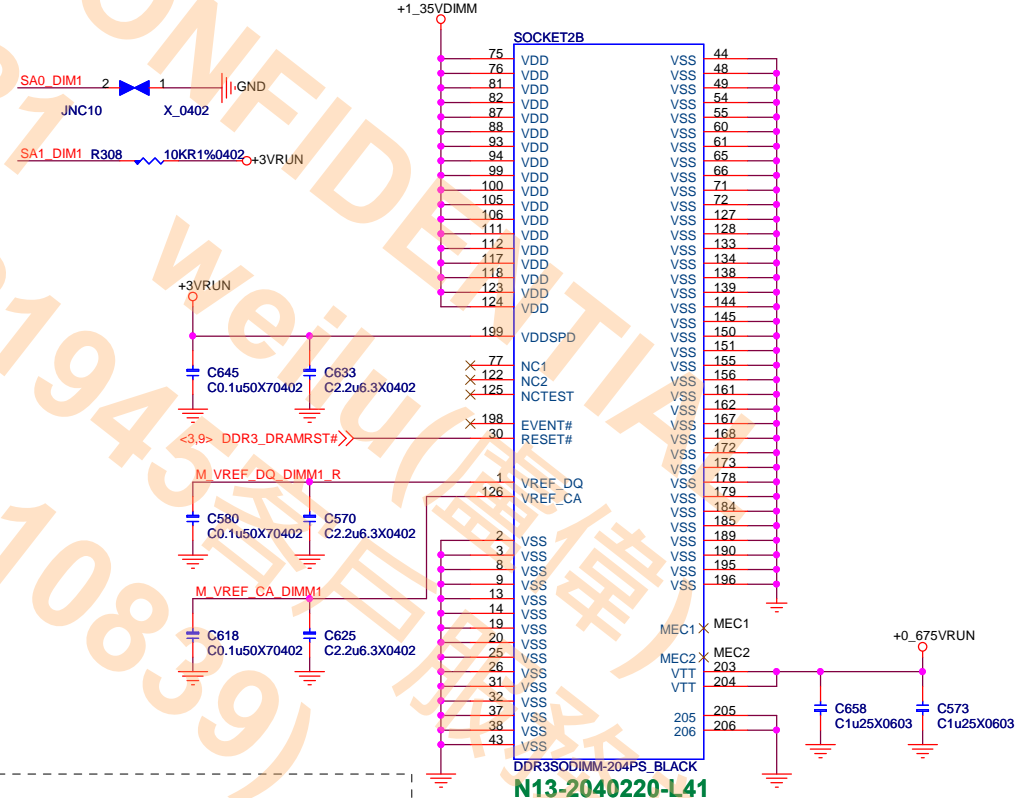
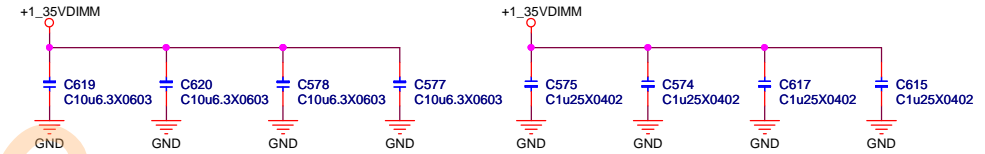
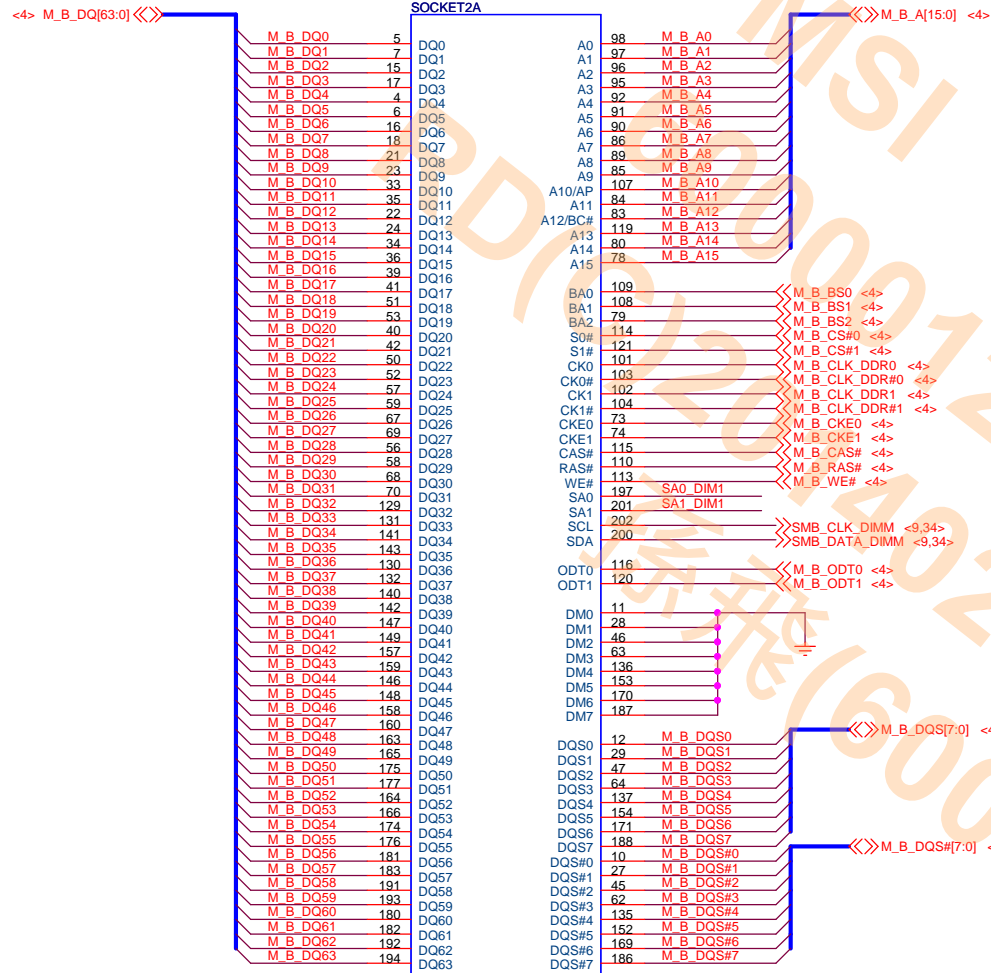
msi		MICRO-STAR INT'L CO.,LTD.	
Title			
CPU-5 (GND)			
Size	Document Number		Rev
	MS-16H2		1.0
Date:	Friday, January 03, 2014		Sheet 8 of 72

SODIMM#A

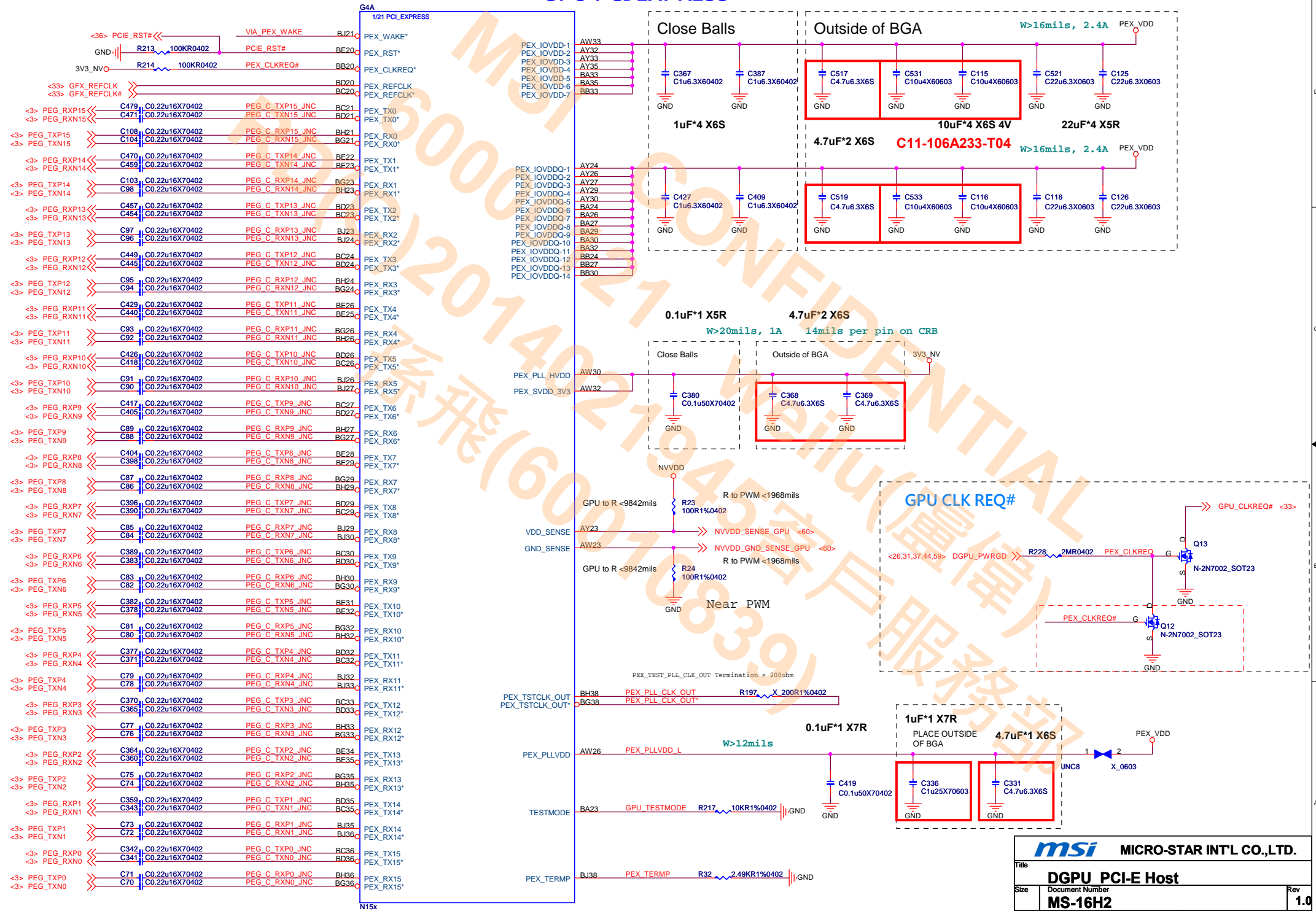
PCB layout for SODIMM#A showing various signal traces, power planes, and component footprints. The layout includes a top section with a +1.35V DIMM power plane, a middle section with signal traces for M_A_BS0, M_A_BS1, M_A_BS2, M_A_CS#0, M_A_CS#1, M_A_CLK_DDR0, M_A_CLK_DDR#0, M_A_CLK_DDR#1, M_A_CKE0, M_A_CKE1, M_A_CAS#, M_A_RAS#, and M_A_WE#, and a bottom section with a +3V RUN power plane. The layout also shows a DIMM connector footprint with pins 1 through 26. The layout is labeled with various component values and footprints, including C651, C635, C6581, C0.1u50X70402, C646, C0.1u50X70402, C657, C0.1u50X70402, and R356, 2R1%0402, CA A, R357, X 0R1%0402, DIMM_SM_VREF, and DIMM_SM_VREF. The layout is also labeled with various signal names, including M_A_BS0, M_A_BS1, M_A_BS2, M_A_CS#0, M_A_CS#1, M_A_CLK_DDR0, M_A_CLK_DDR#0, M_A_CLK_DDR#1, M_A_CKE0, M_A_CKE1, M_A_CAS#, M_A_RAS#, M_A_WE#, M_A_ODT0, M_A_ODT1, M_A_DQS[7:0], and M_A_DQS#[7:0]. The layout is also labeled with various power and ground planes, including +1.35V DIMM, +3V RUN, and DIMM_SM_VREF.



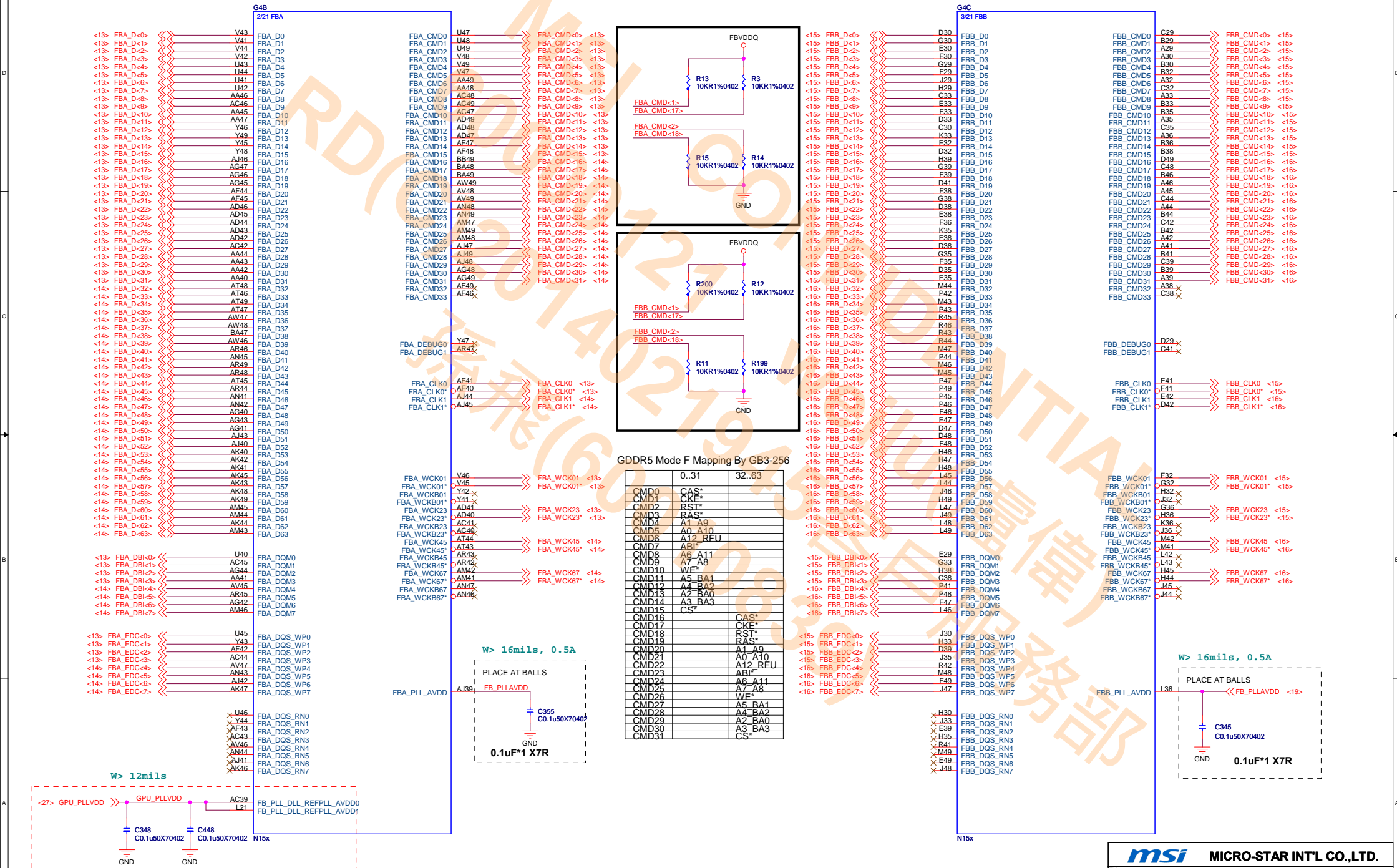
SODIMM#B



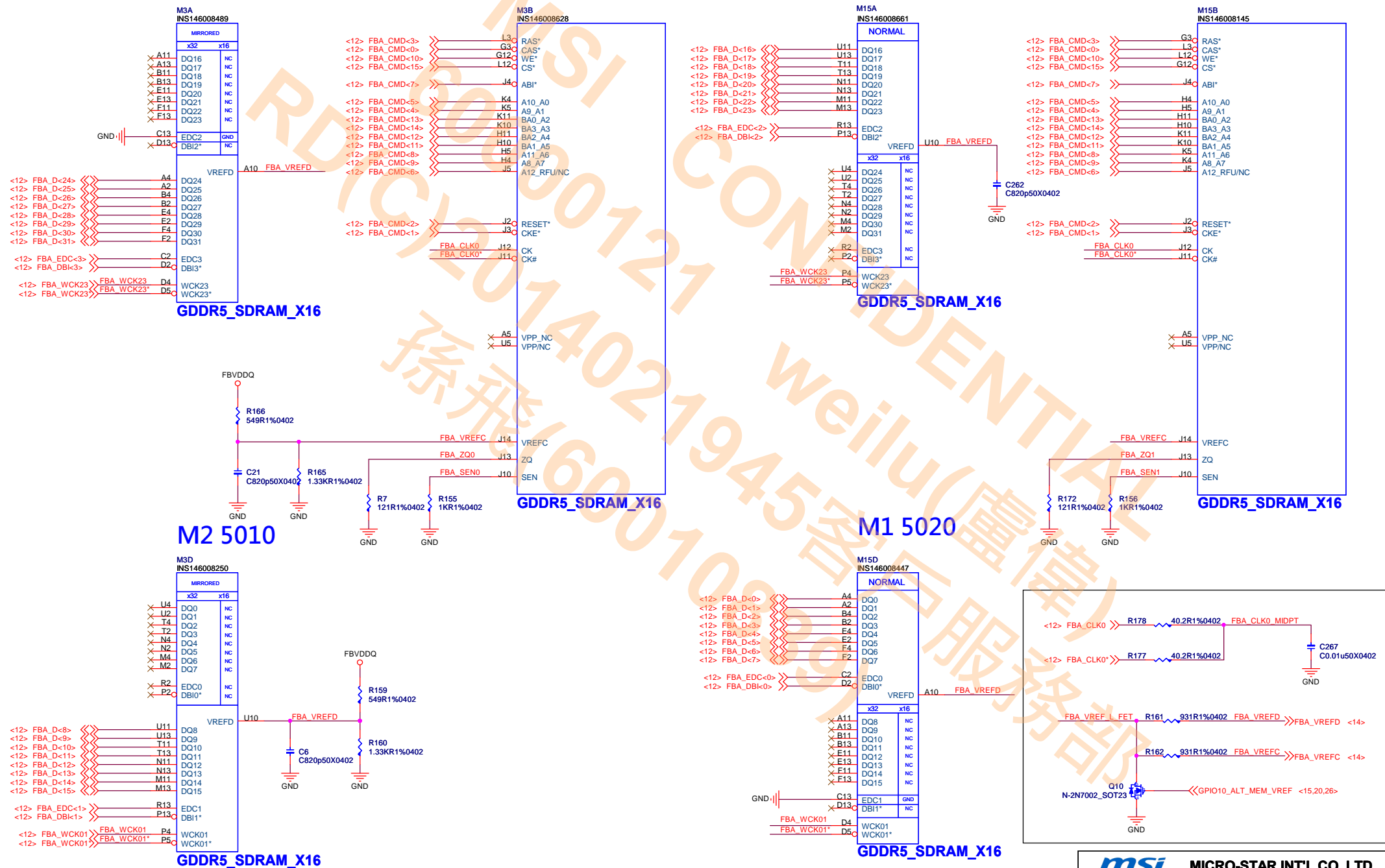
GPU PCI EXPRESS



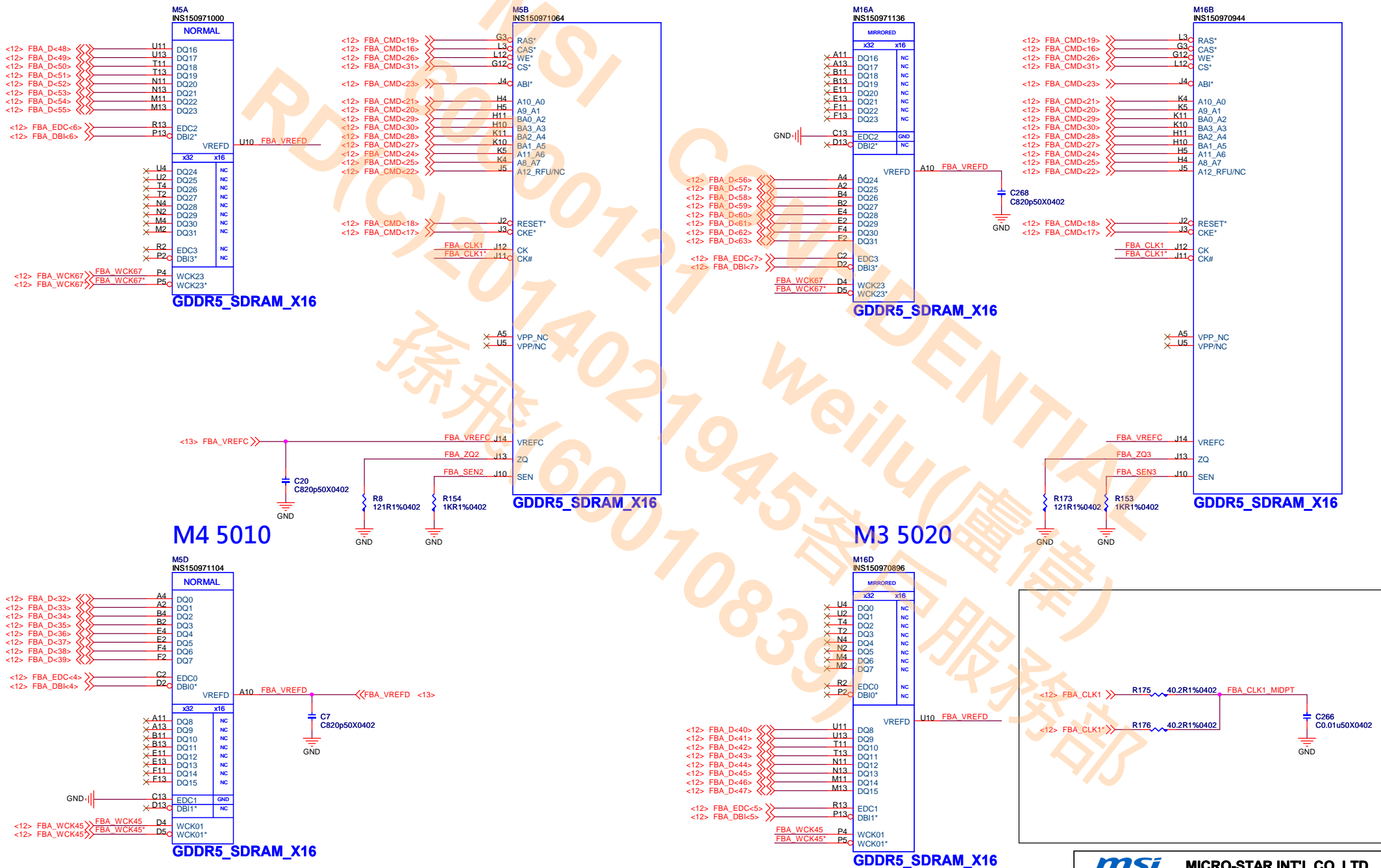
GPU Frame Buffer Partition A/B



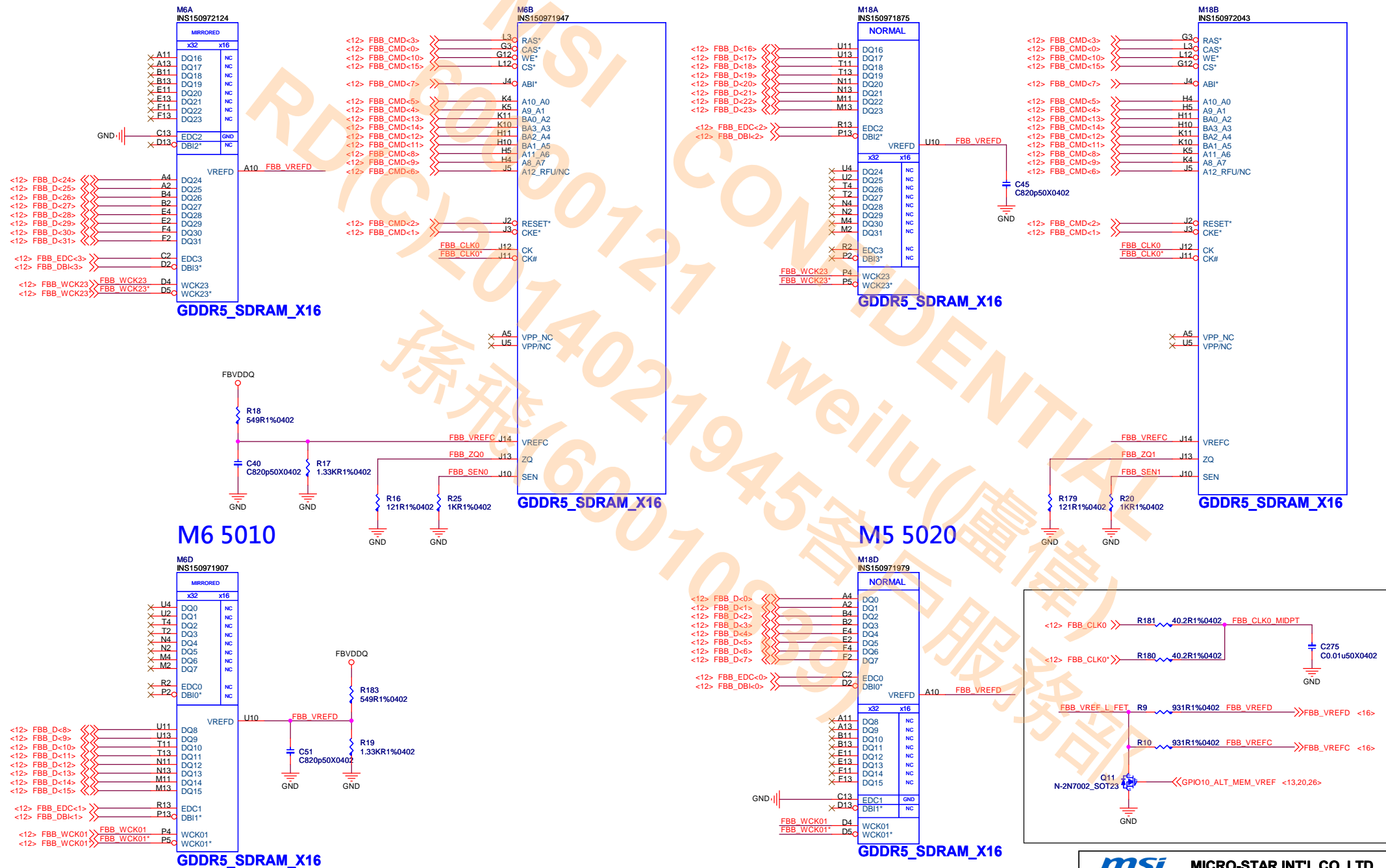
DGPU_GDDR5 FrameBuffer A0



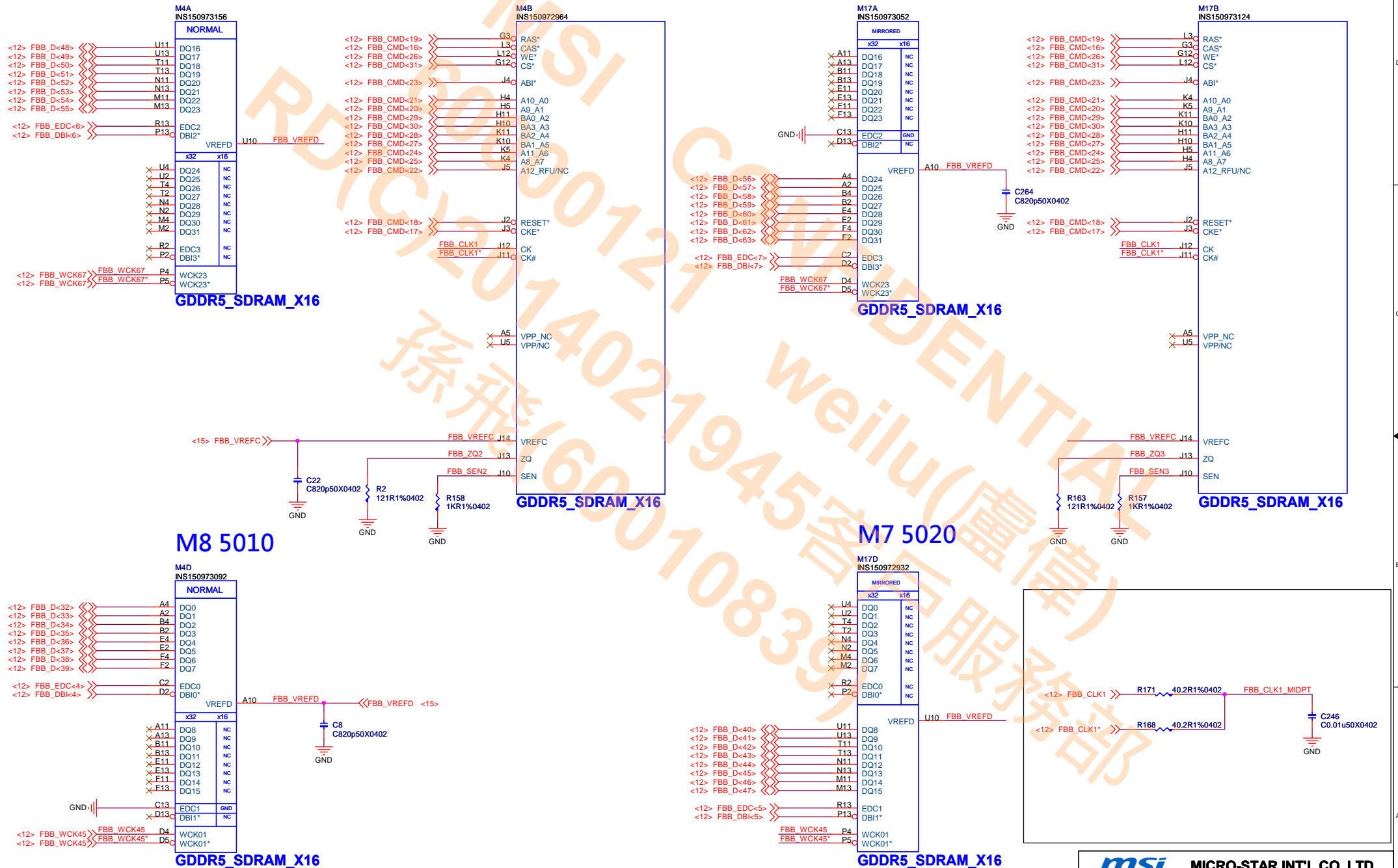
DGPU_GDDR5 FrameBuffer A1



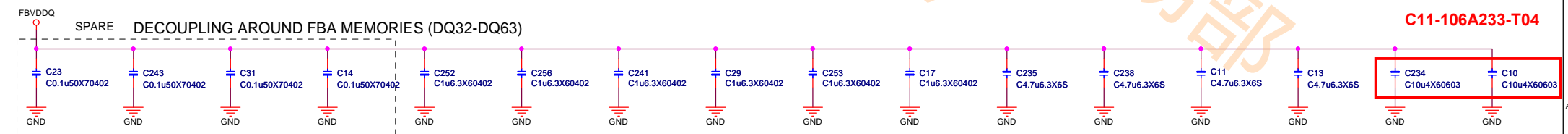
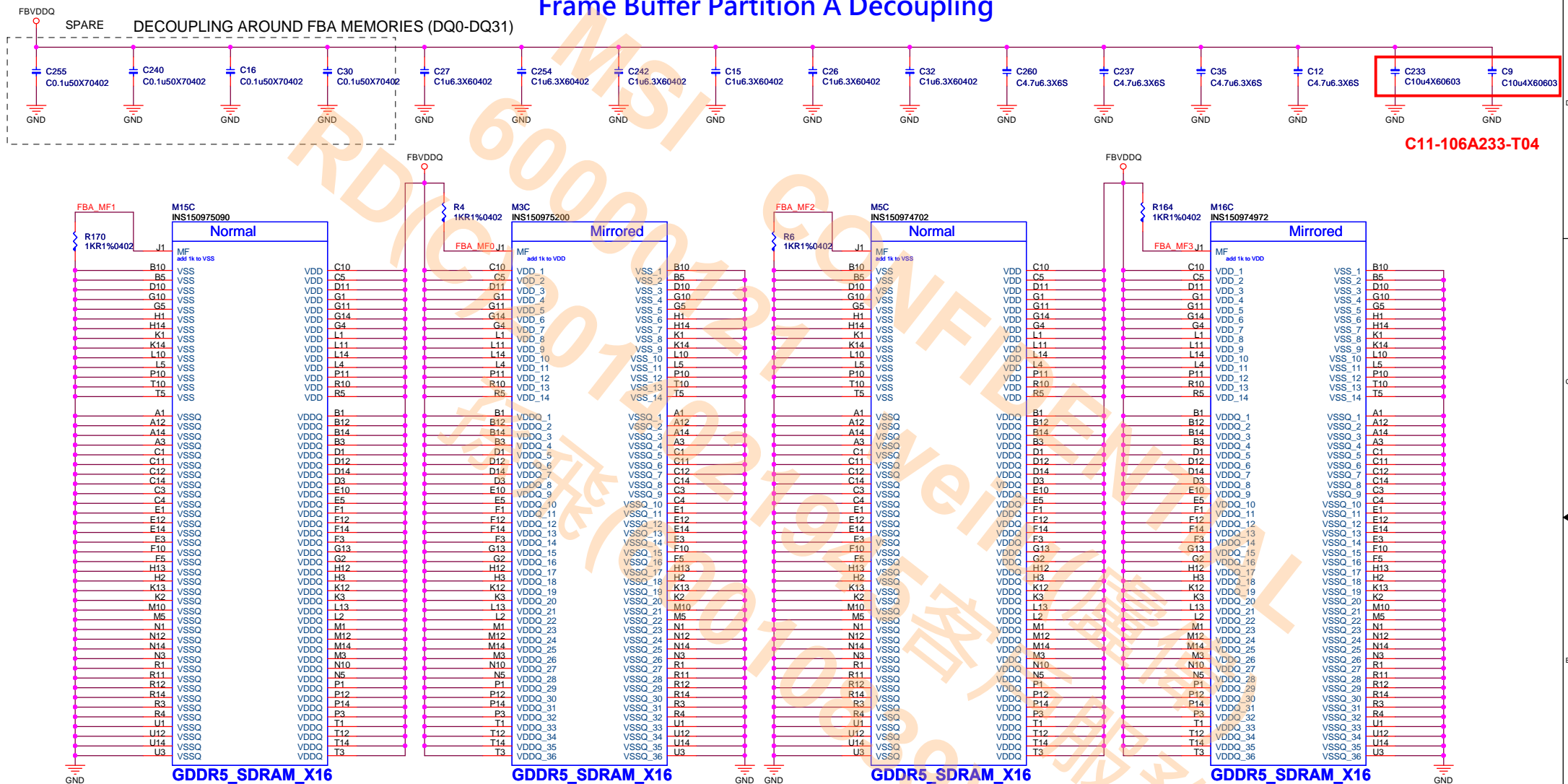
DGPU_GDDR5 FrameBuffer B0



DGPU_GDDR5 FrameBuffer B1



Frame Buffer Partition A Decoupling



FBVDDQ

SPARE

DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)

C272
C0.1u50X70402

C269
C0.1u50X70402

C24
C0.1u50X70402

C19
C0.1u50X70402

C271
C1u6.3X60402

C250
C1u6.3X60402

C245
C1u6.3X60402

C42
C1u6.3X60402

C43
C1u6.3X60402

C39
C1u6.3X60402

C270
C4.7u6.3X6S

C261
C4.7u6.3X6S

C41
C4.7u6.3X6S

C36
C4.7u6.3X6S

C257
C10u4X60603

C492
C10u4X60603

[illegible]

FBVDDQ SPARE DECOUPLING AROUND FBB MEMORIES (DQ32-DQ63)

C236 C0.1u50X70402 GND

C251 C0.1u50X70402 GND

C62 C0.1u50X70402 GND

C332 C0.1u50X70402 GND

C347 C1u6.3X60402 GND

C249 C1u6.3X60402 GND

C244 C1u6.3X60402 GND

C18 C1u6.3X60402 GND

C239 C1u6.3X60402 GND

C28 C1u6.3X60402 GND

C263 C4.7u6.3X6S GND

C335 C4.7u6.3X6S GND

C37 C4.7u6.3X6S GND

C64 C4.7u6.3X6S GND

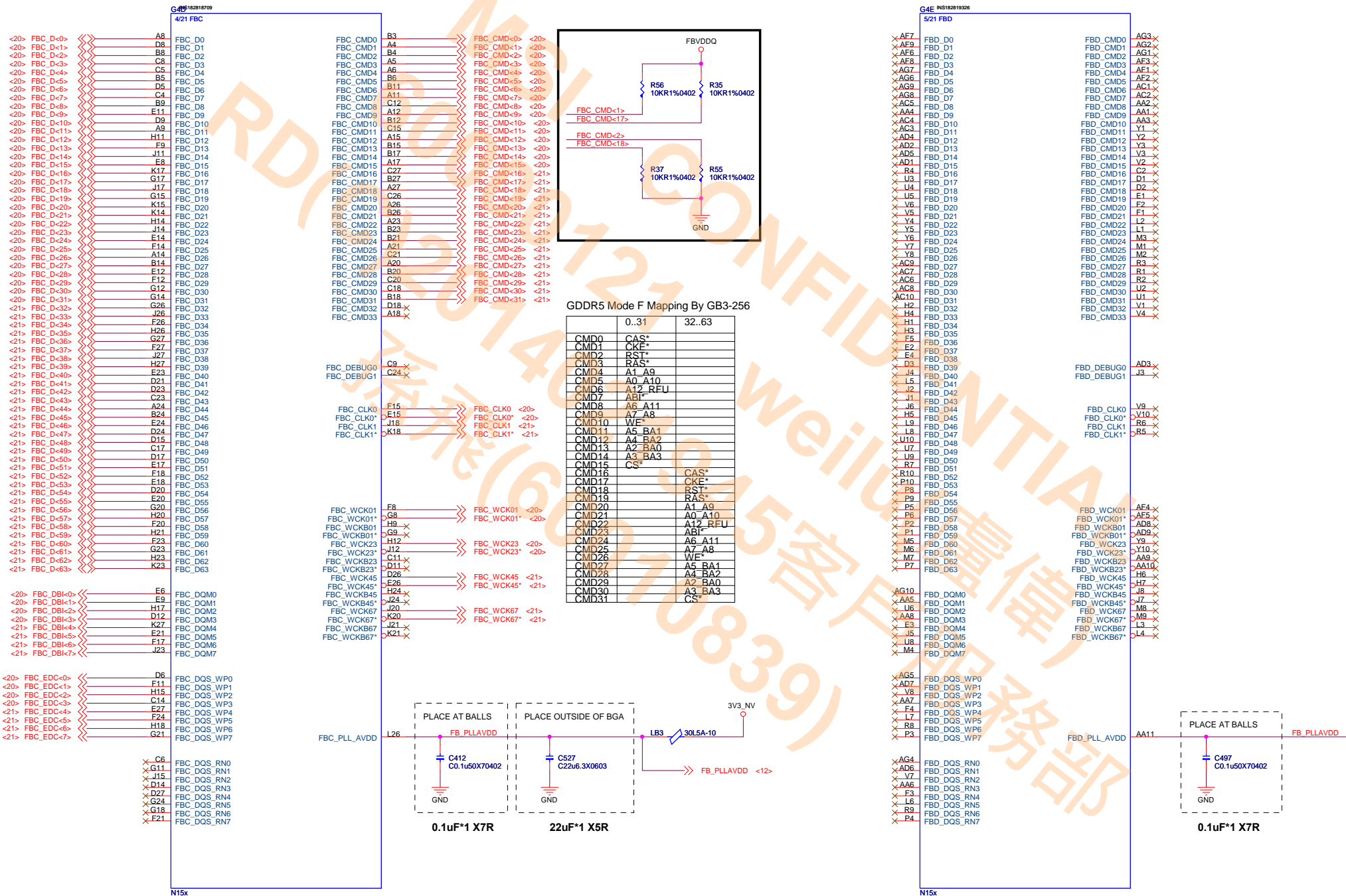
C288 C10u4X60603 GND

C258 C10u4X60603 GND

Change Page for Layout C11-106A233-T04

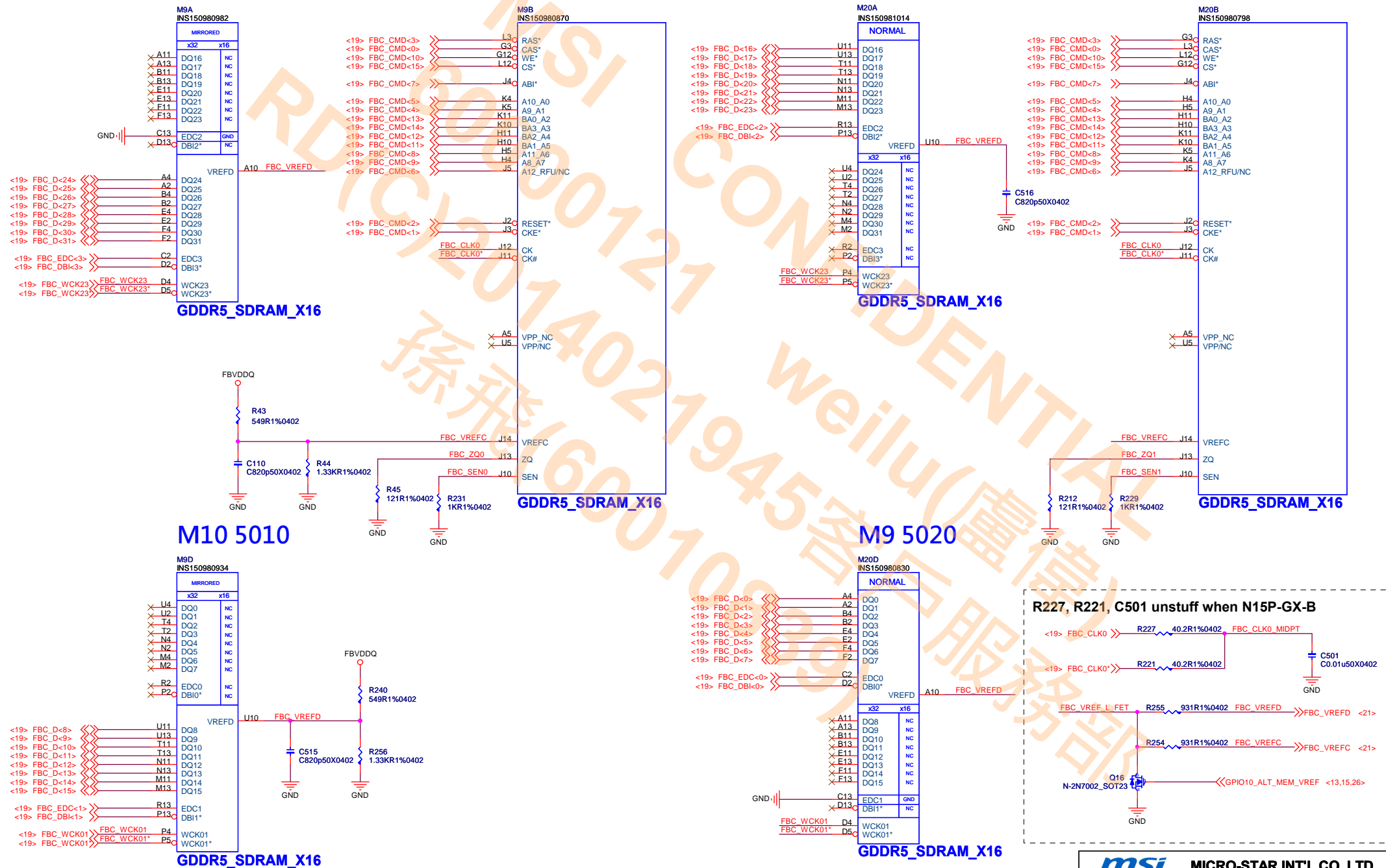
C11-106A233-T04

GPU Frame Buffer Partition C/D

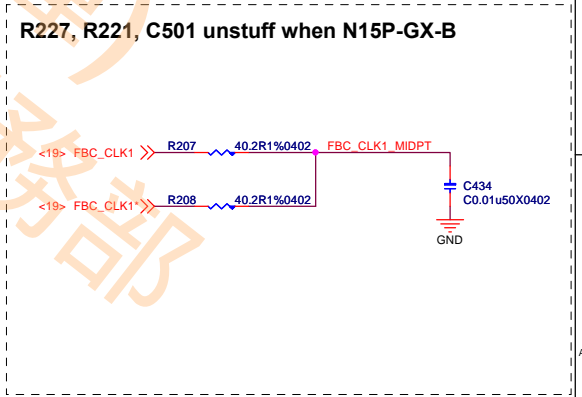


DGPU_GDDR5 FrameBuffer C0

(N15P-GX-B ALL unstuff)

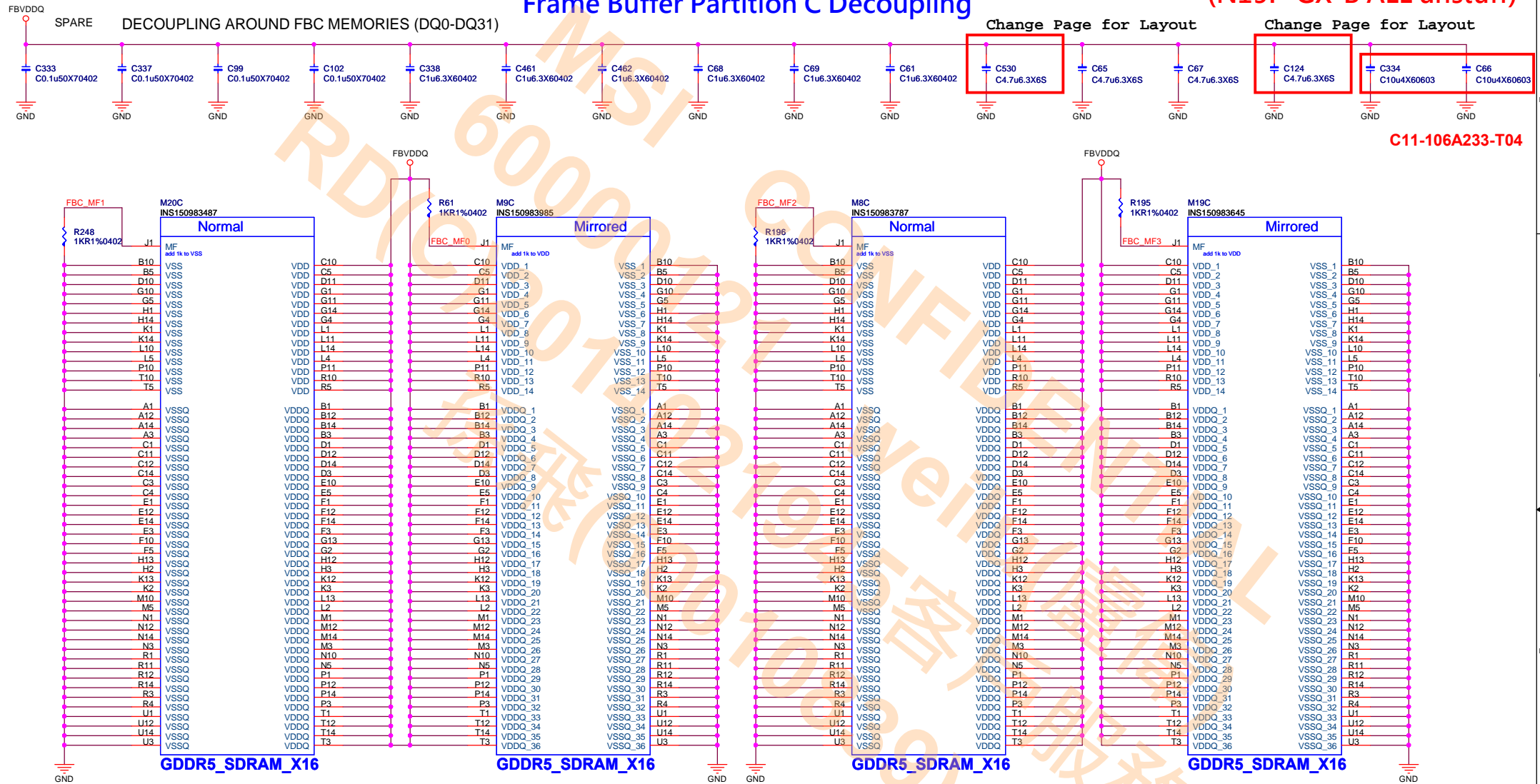


(N15P-GX-B ALL unstuff)

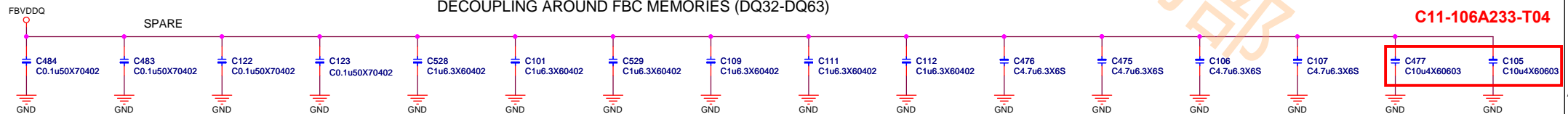


Frame Buffer Partition C Decoupling

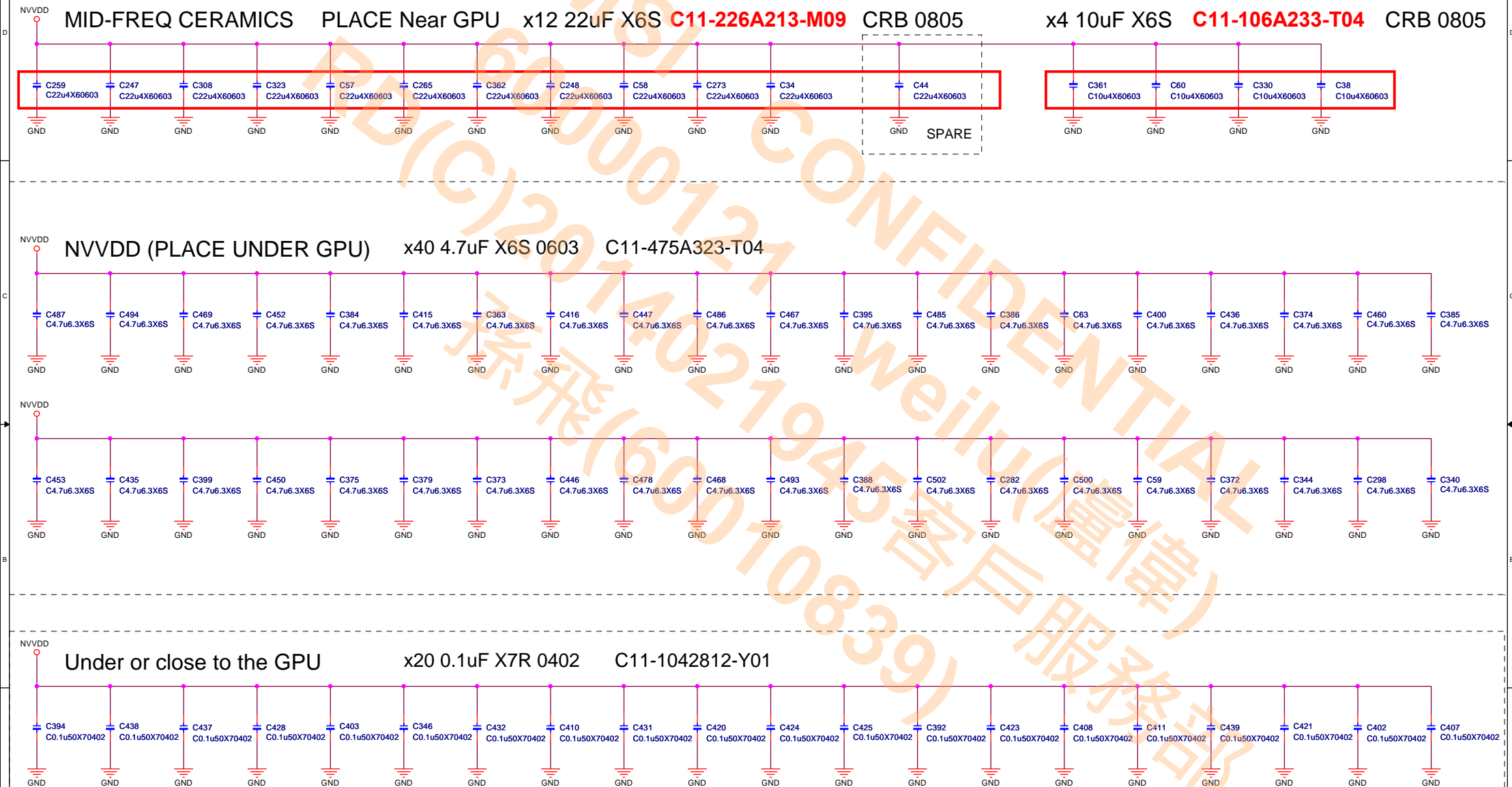
(N15P-GX-B ALL unstuff)



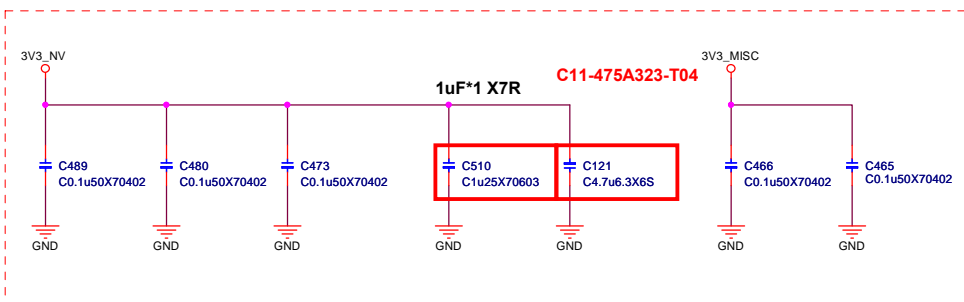
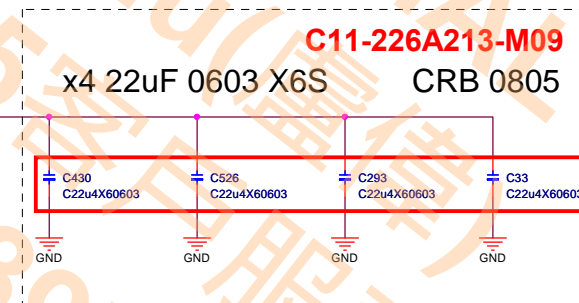
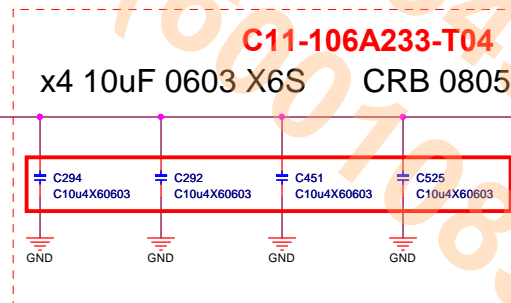
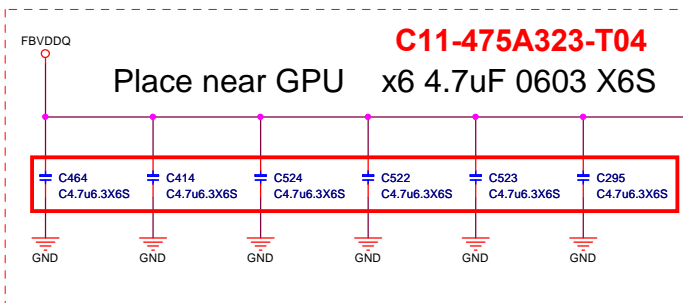
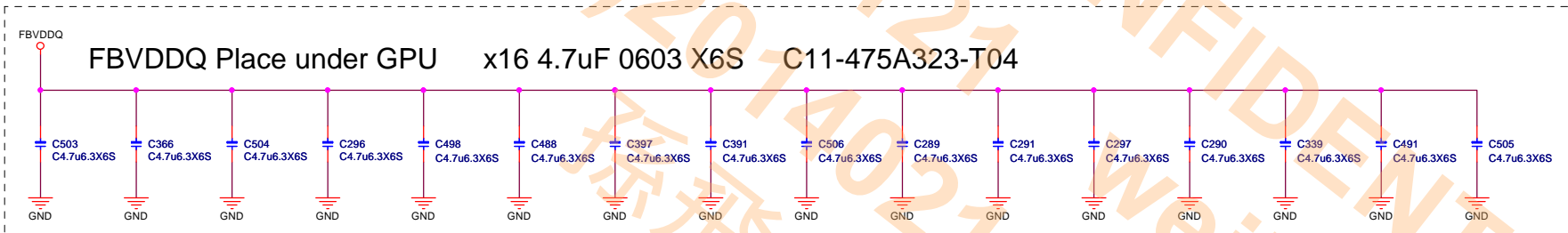
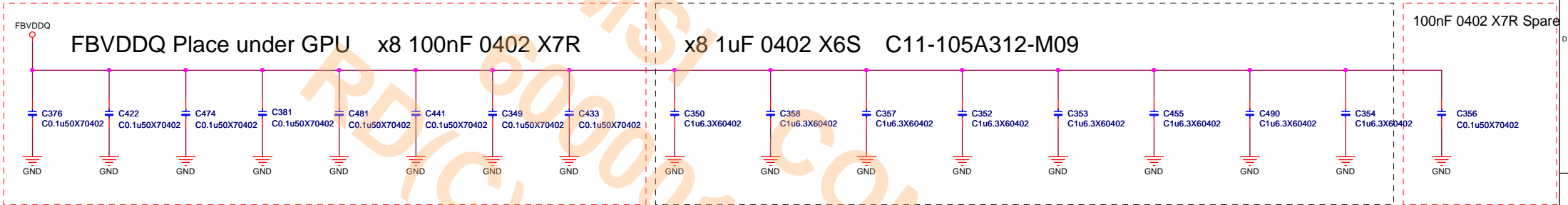
DECOUPLING AROUND FBC MEMORIES (DQ32-DQ63)



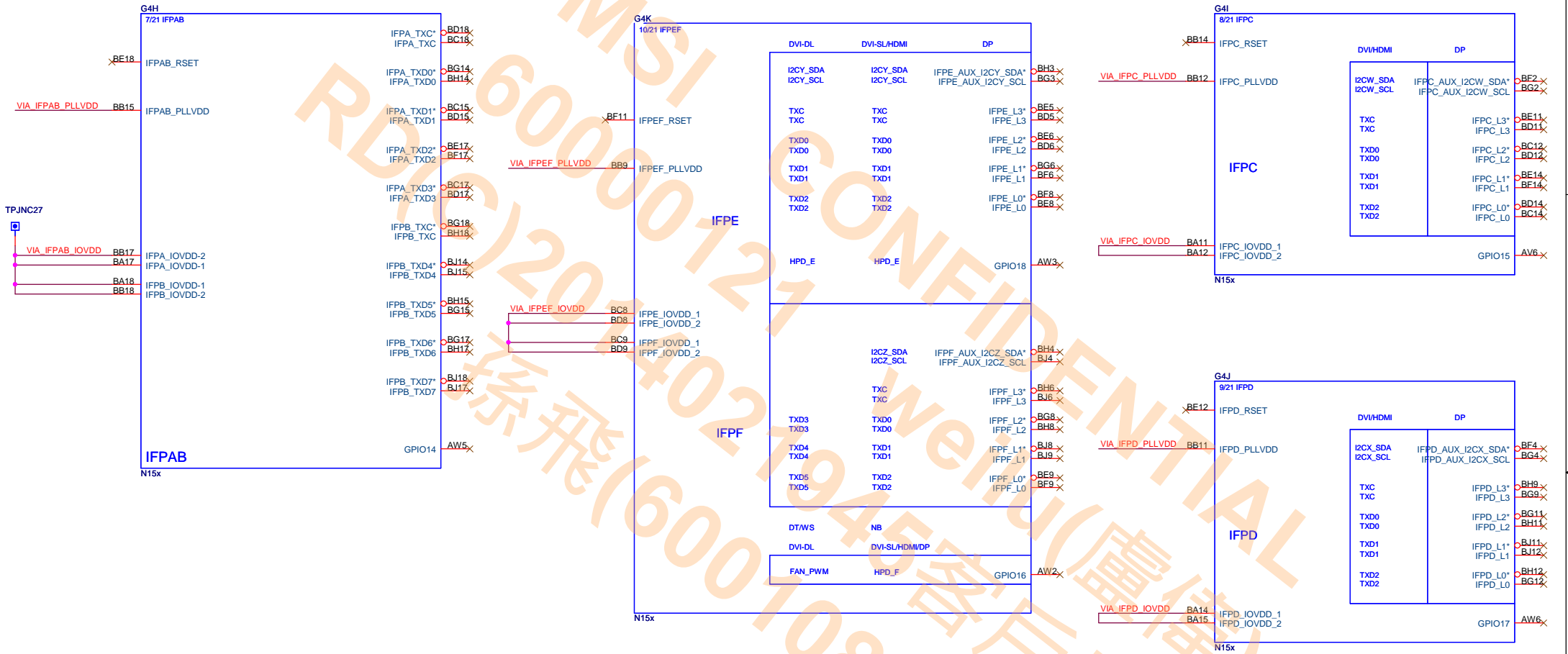
GPU DECOUPLING A



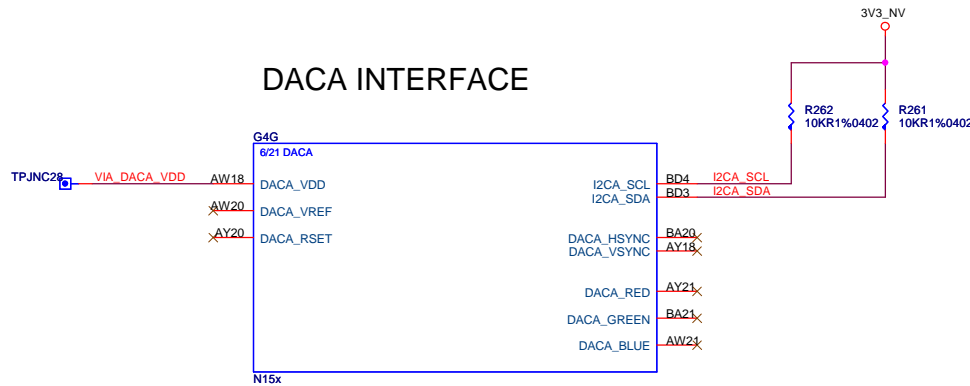
GPU DECOUPLING B



DACA,Display IF



DACA INTERFACE



The schematic diagram illustrates the I2C and SMBus interface for the DGPU. It shows the connection of the GPU's I2C and SMBus lines to various components, including the MOS gate, thermal sensors, and voltage regulators.

Key Components and Connections:

- MOS Gate:** The MOS gate is controlled by the `FB_CLAMP` and `FB_CLAMP_REQ#` signals. The gate is connected to `+3VRUN` and `3V3_NV` through resistors `R268` and `R246`. The MOS gate is labeled `Q15` and `NN-2N7002DW-7-F`.
- SMBus Interface:** The SMBus interface is connected to the GPU's `SMB_CLK_GPU` and `SMB_DATA_GPU` lines. The SMBus lines are connected to the GPU's `SMB_CLK_EC` and `SMB_DATA_EC` lines through resistors `R276` and `R269`.
- Thermal Sensors:** The thermal sensors are connected to the GPU's `I2CC_SCL` and `I2CC_SDA` lines. The thermal sensors are labeled `BF3`, `BD2`, `BD1`, `BB5`, and `BB4`.
- Voltage Regulators:** The voltage regulators are connected to the GPU's `I2CB_SCL` and `I2CB_SDA` lines. The voltage regulators are labeled `AT9`, `AT7`, `AV1`, `AW4`, `AW1`, `AT4`, `AT1`, `AT10`, `AV7`, `AV2`, `AV4`, and `AT5`.

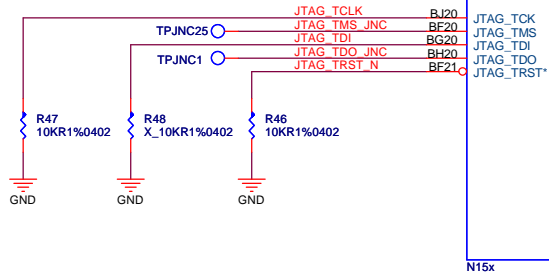
Legend:

- `<29,31,44> FB_CLAMP`: (From EC)
- `<44> FB_CLAMP_REQ#`: (To EC)
- `<44> SMB_CLK_EC`
- `<44> SMB_DATA_EC`

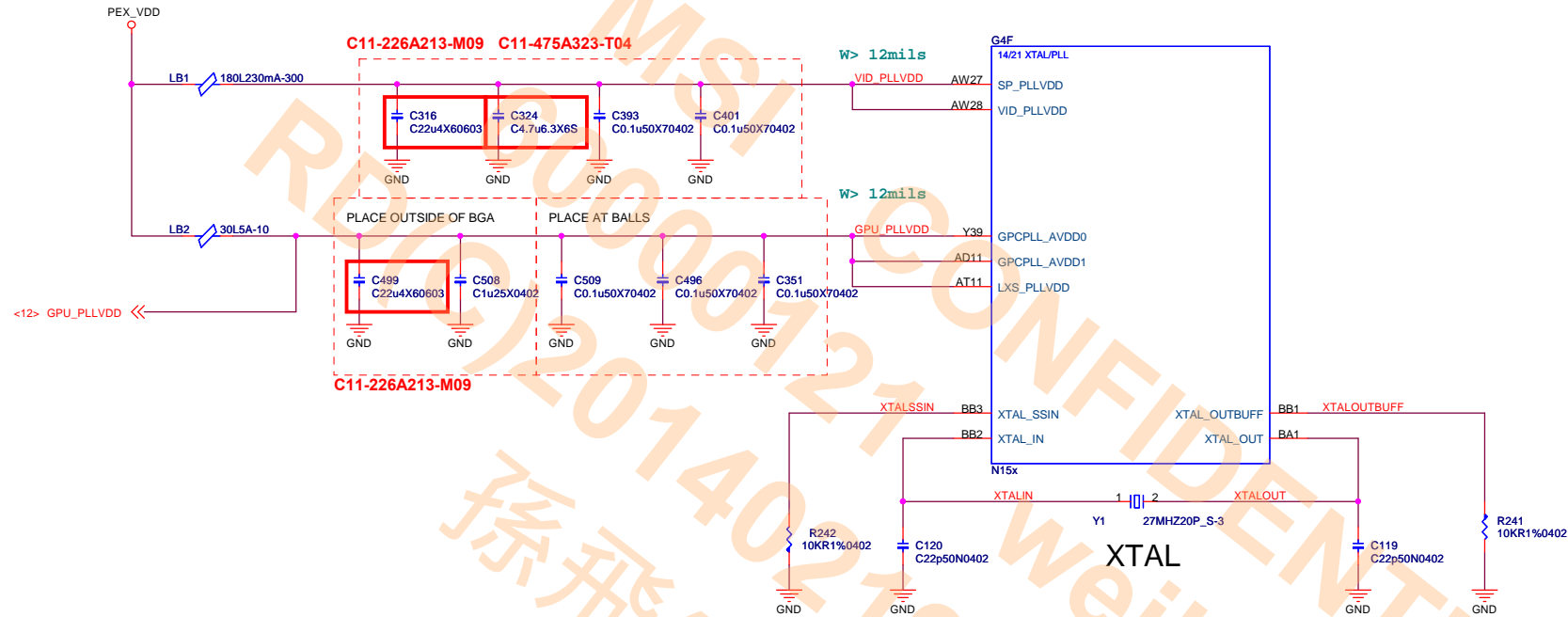
Component Values:

- `R268`: 10K R1%0402
- `R246`: 10K R1%0402
- `R247`: 10K R1%0402
- `R276`: 2.2K R1%0402
- `R269`: 2.2K R1%0402
- `R67`: 2.2K R1%0402
- `R68`: 2.2K R1%0402
- `R238`: 10K R1%0402
- `R245`: 10K R1%0402
- `R63`: 33R0402
- `R64`: 33R0402
- `R57`: 10K R1%0402
- `R58`: 10K R1%0402
- `R222`: 10K R1%0402
- `R239`: 10K R1%0402
- `R400`: 10K R1%0402
- `R243`: 10K R1%0402
- `R225`: 100K R0402

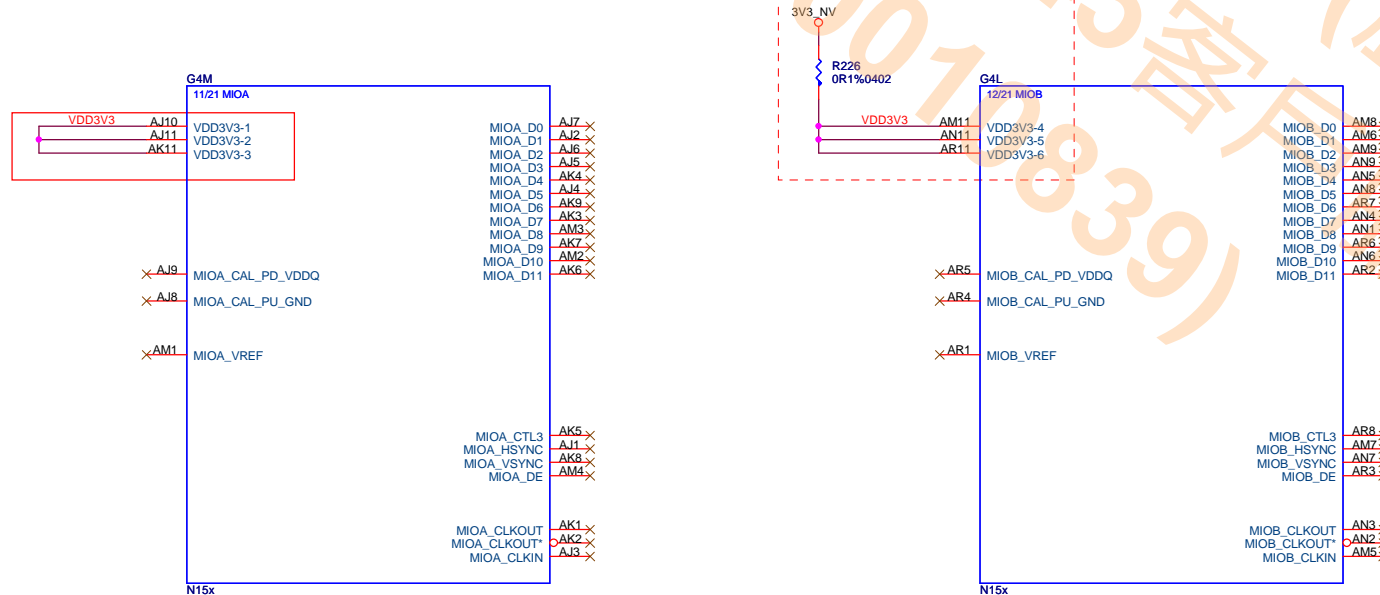
GPIO	I/O	Function
0	OUT	PWM_VID
1	IN	FB_CLAMP_MON
2	OUT	FB_CLAMP_MON_TGL_REQ
3	IN	OC_WARN
4	N/A	Reserved
5	N/A	Reserved
6	OUT	PSI
7	OUT	LCD_PWM
8	OUT	OVERT
9	I/O	ALERT
10	OUT	MEM_VREF_CTL
11	OUT	LCD_VCC
12	IN	PWM_LEVEL
13	OUT	LCD_BLEN
14	IN	HPD_AB
15	IN	HPD_C
16	IN	HPD_F or HPD_B
17	IN	HPD_D
18	IN	HPD_E
19	OUT	3DVision
20	N/A	Reserved
21	I/O	RASTER_SYNC
22	IN	SWAP_RDY
23	N/A	Reserved
24	OUT	MEM_VDD_CTL



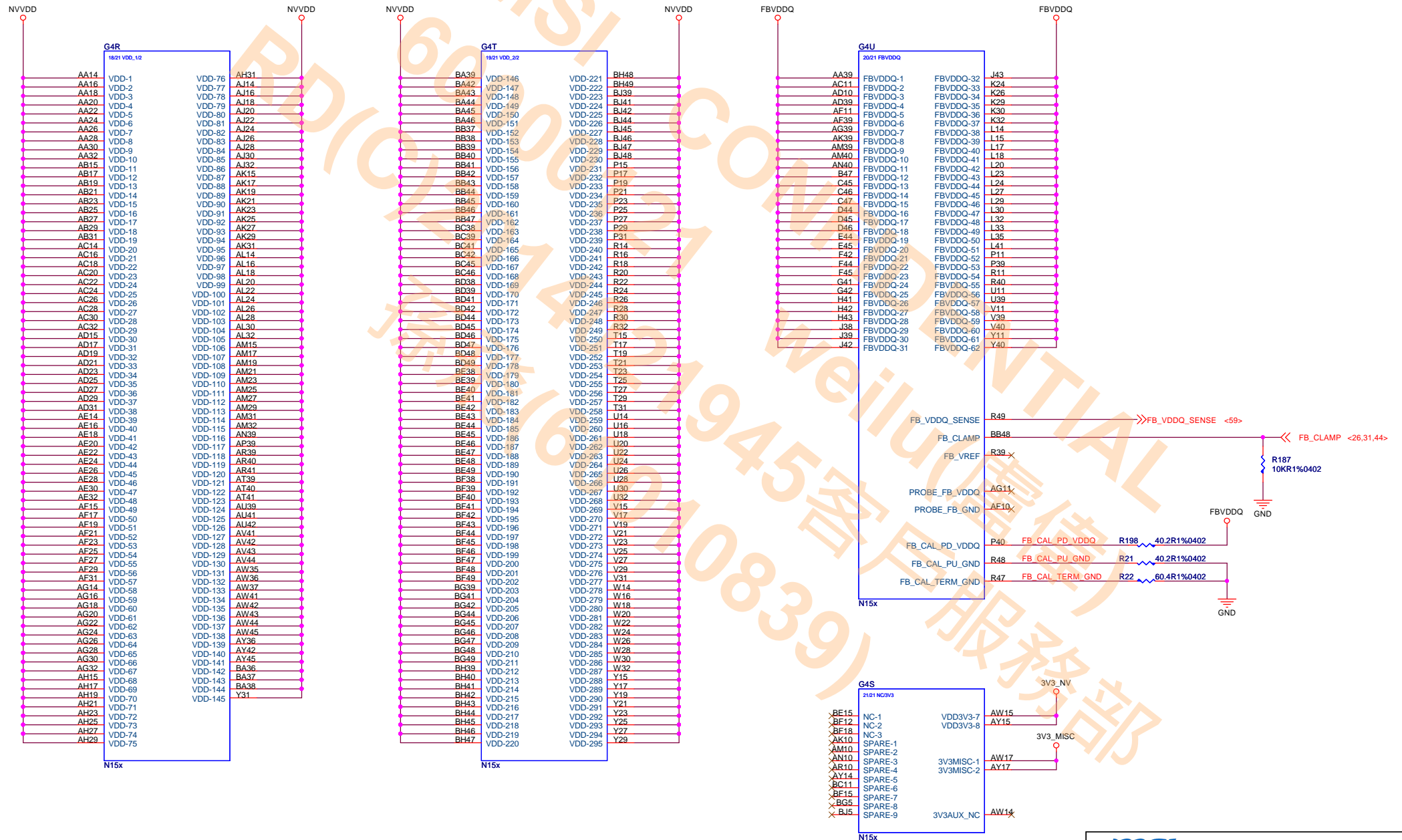
DGPU MIO & XTAL



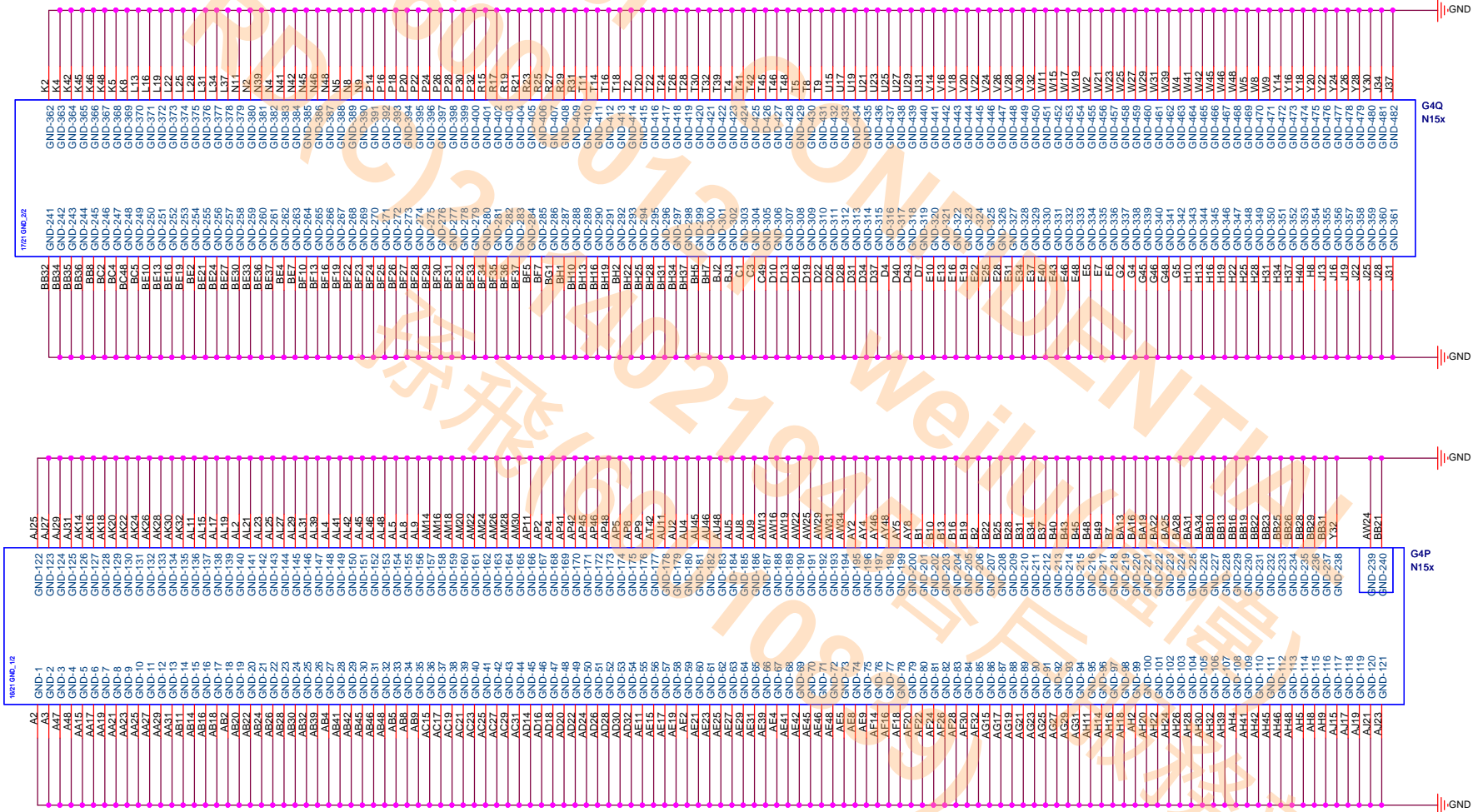
Multi-use IO(MIO) Interface



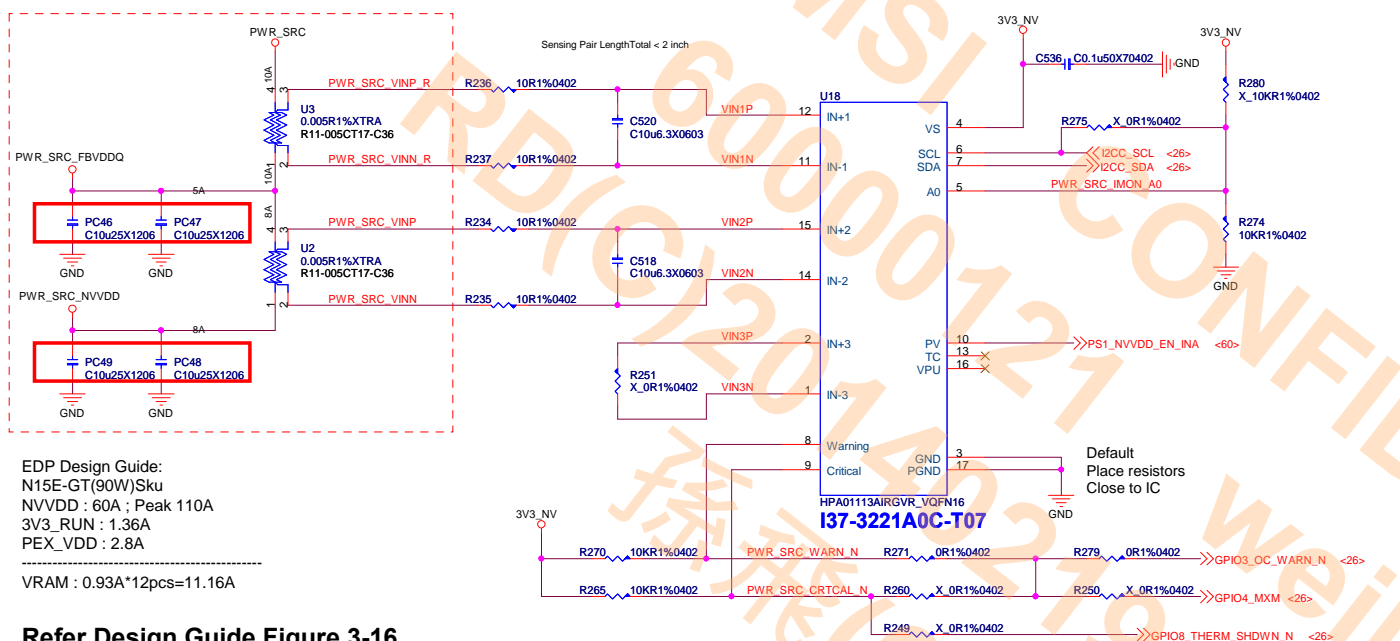
GPU NVVDD, FBVDDQ



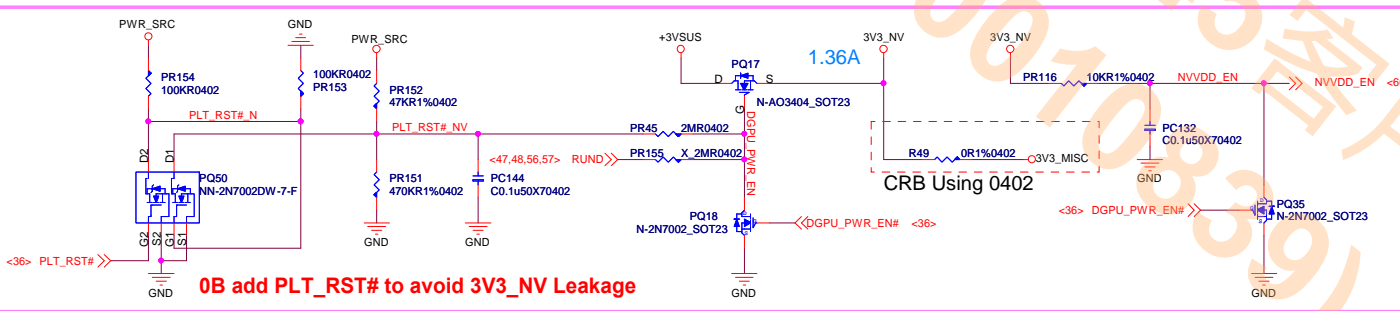
DGPU GND



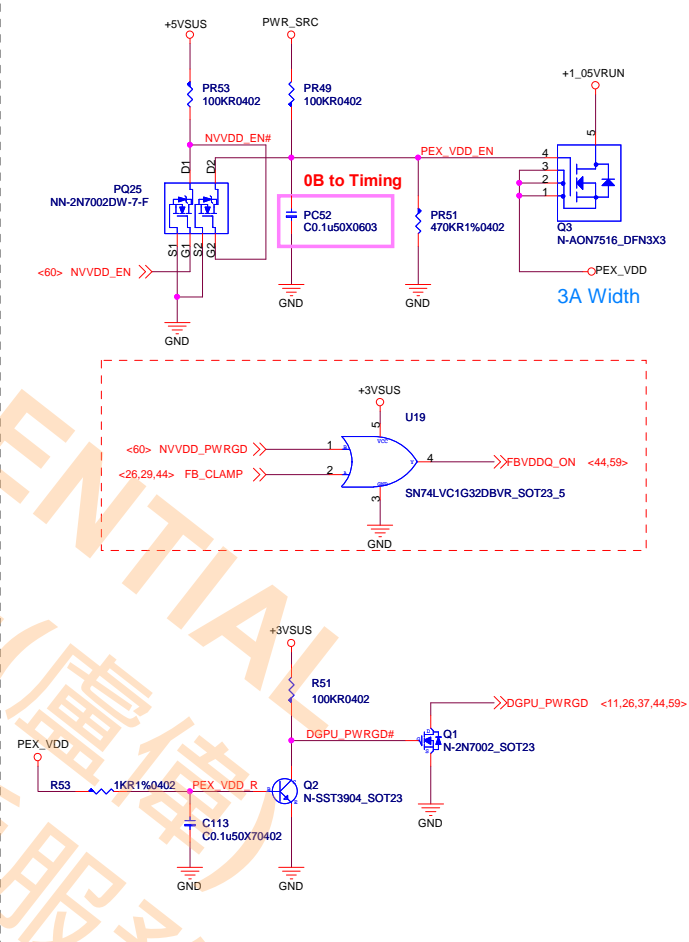
DGPU_Power Control



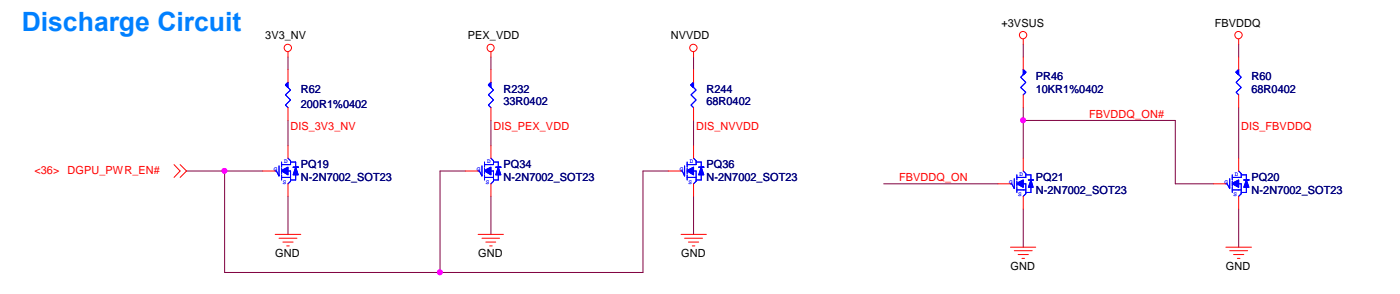
nVIDIA Power Sequence Control 3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD



PEX_VDD

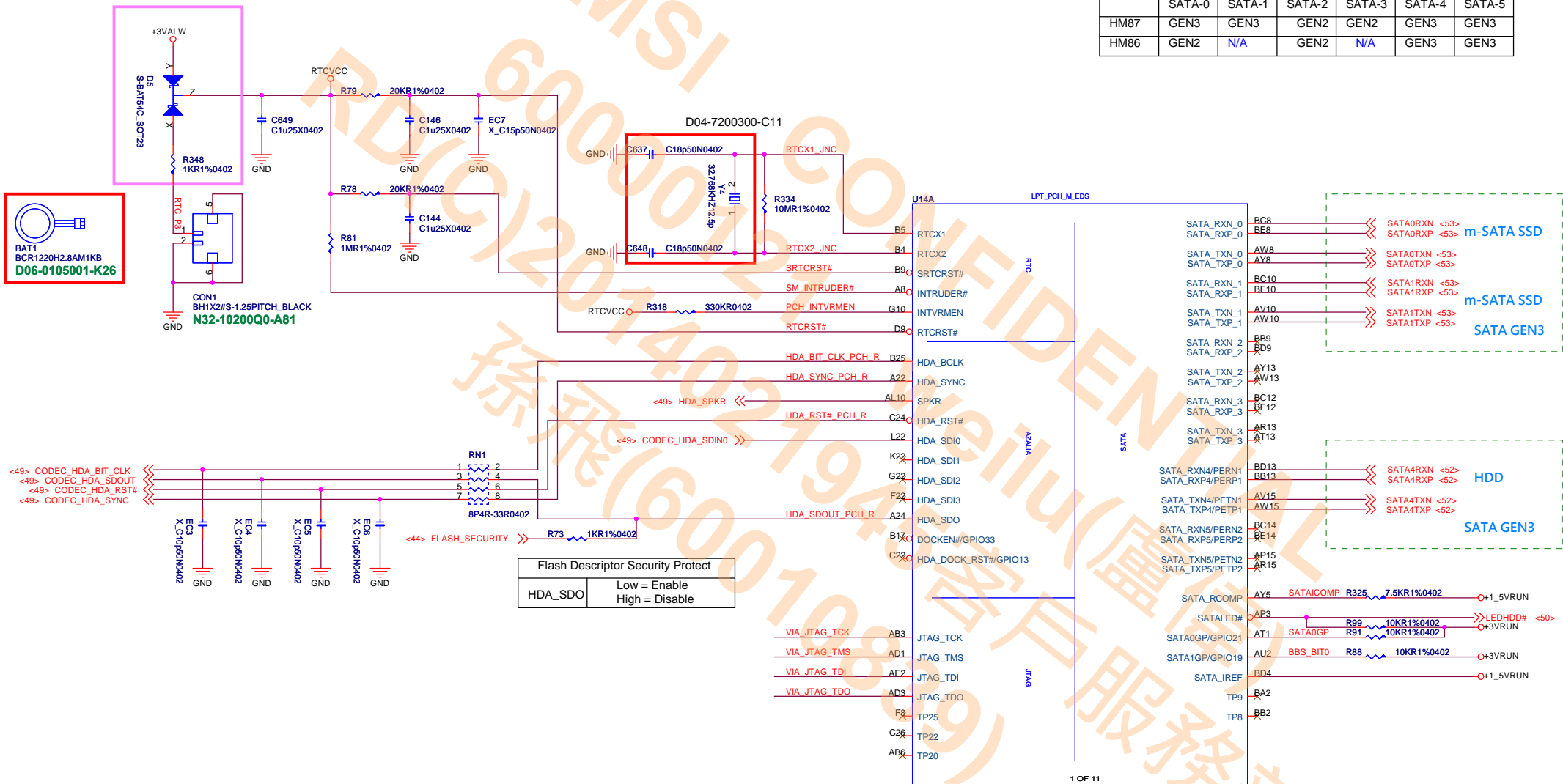


Discharge Circuit



Lynx Point (HDA/JTAG/SATA)

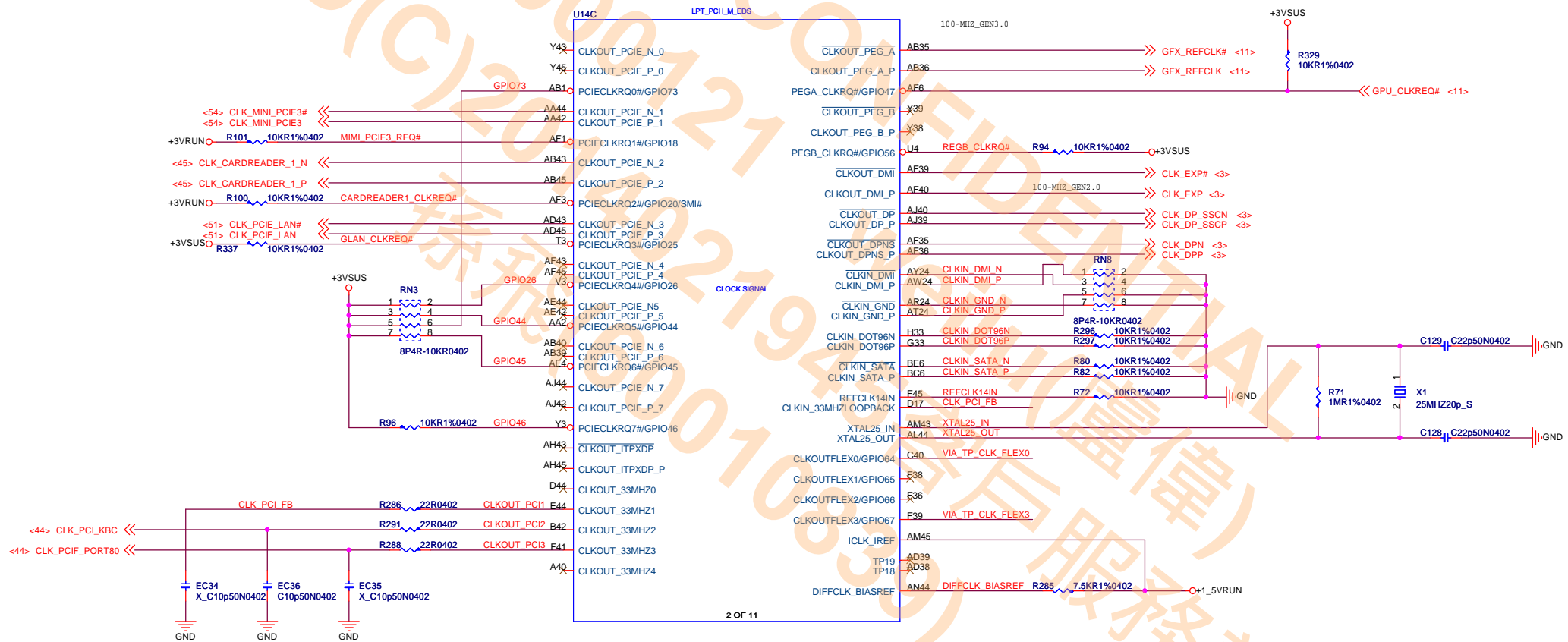
SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



SPK The Signal has a weak internal pull-down
Note: the internal pull-down is disabled after PLTRST# deasserts.
If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
(Panther Point will disable the TCO Timer system reboot feature)

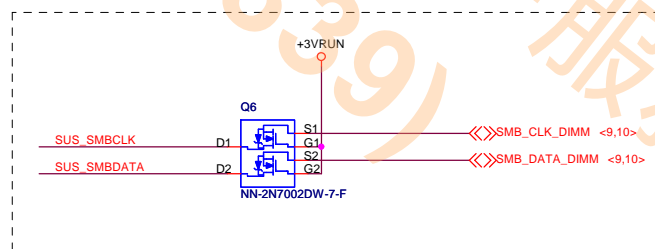
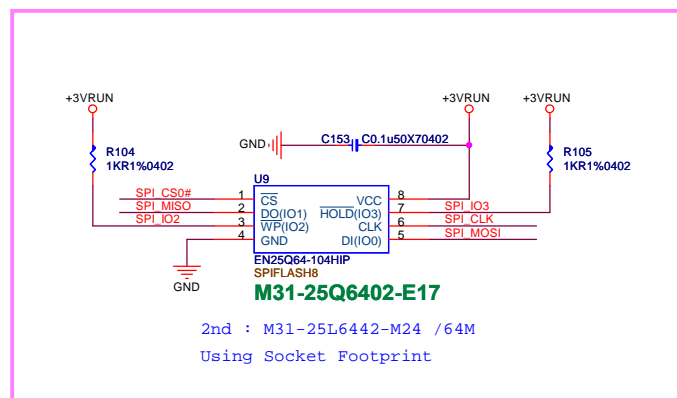
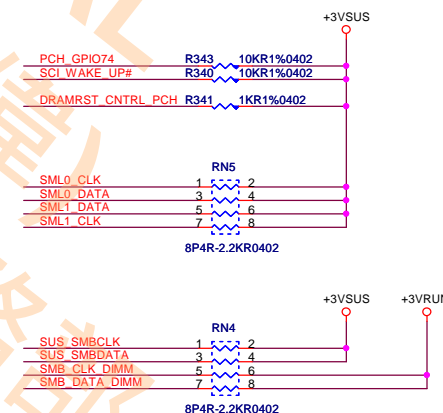
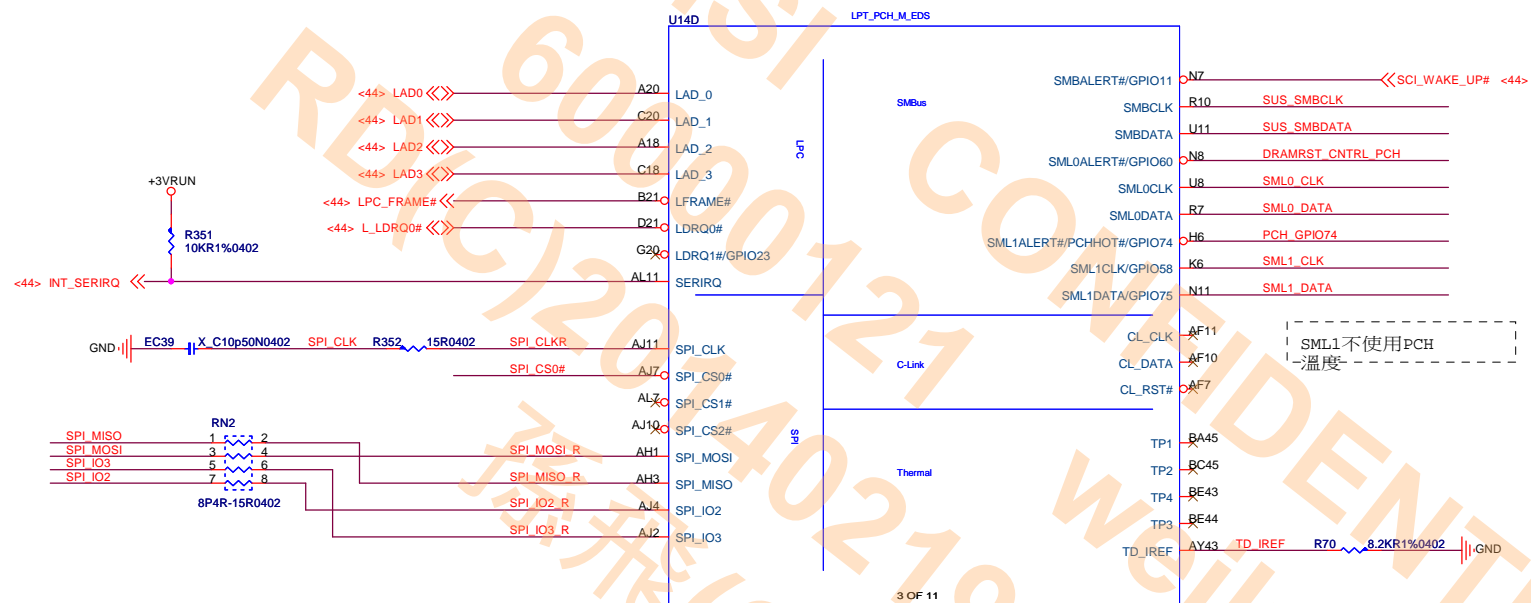
Lynx Point (Clock)

PCIe devices or add-in cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k Ω \pm 10% external pull-up resistor instead of No Connect.
Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

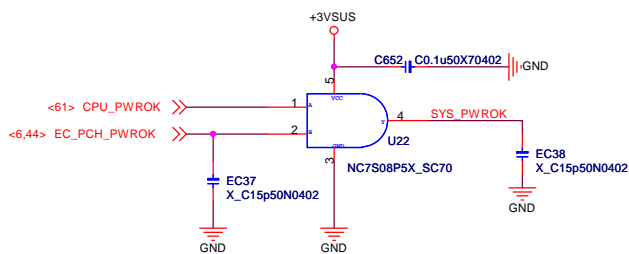
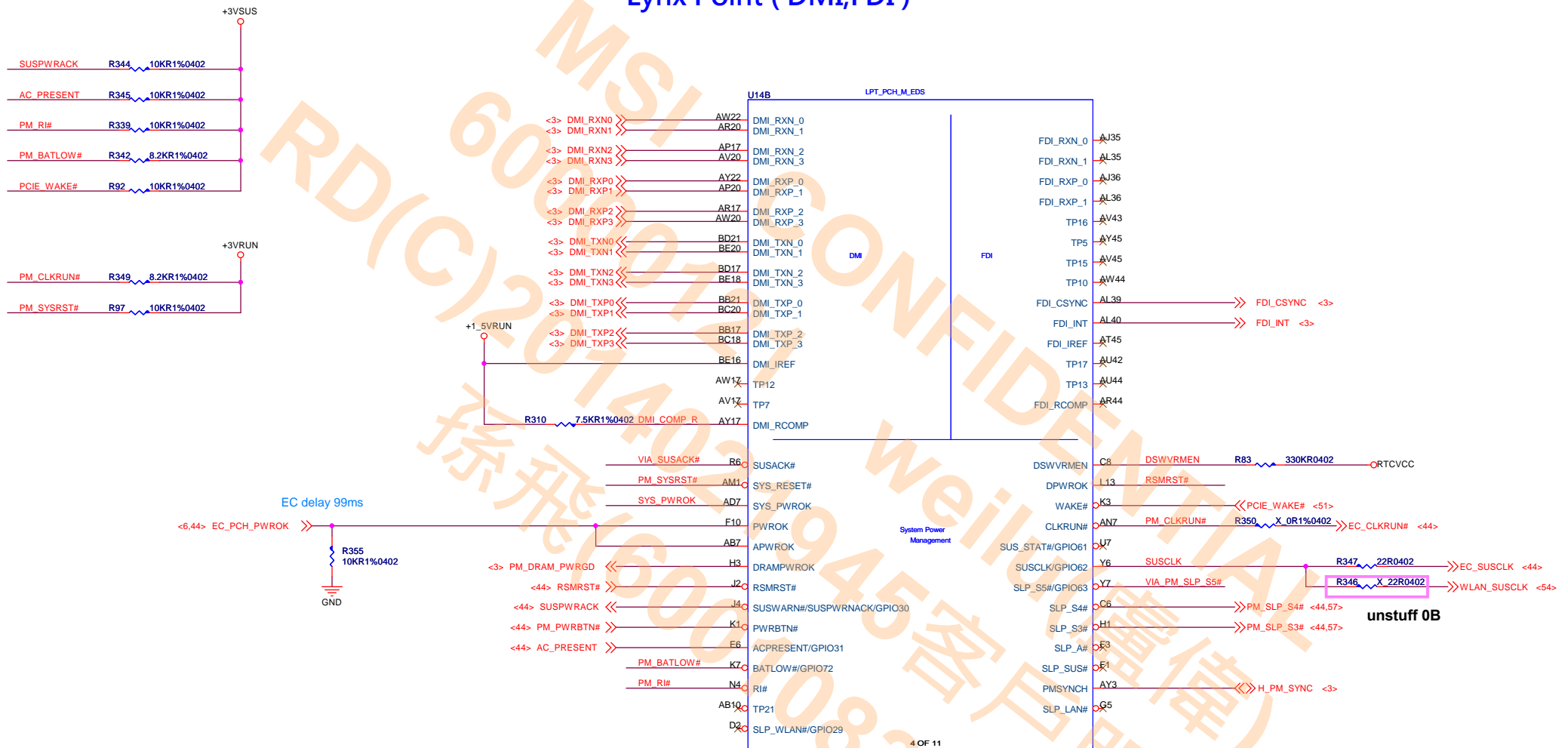


The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

Lynx Point (LPC,SMBUS)



Lynx Point (DMI,FDI)

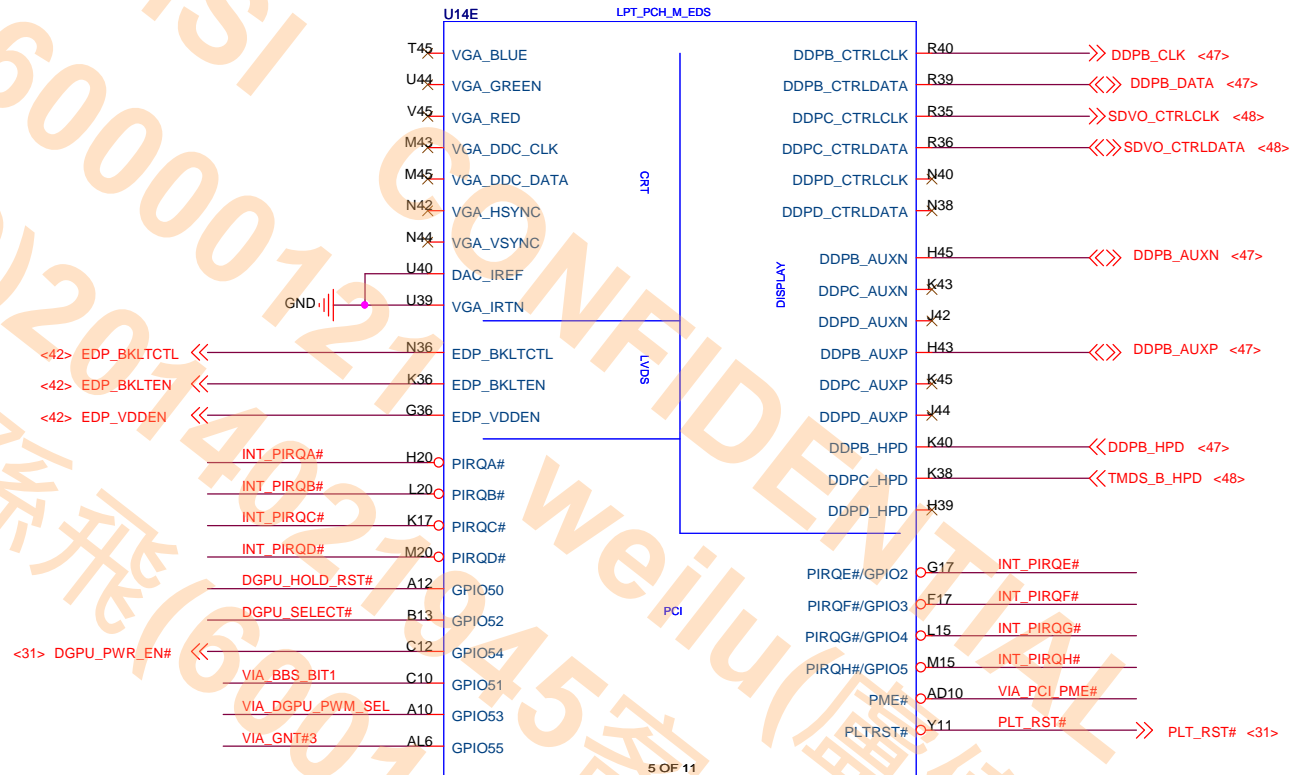
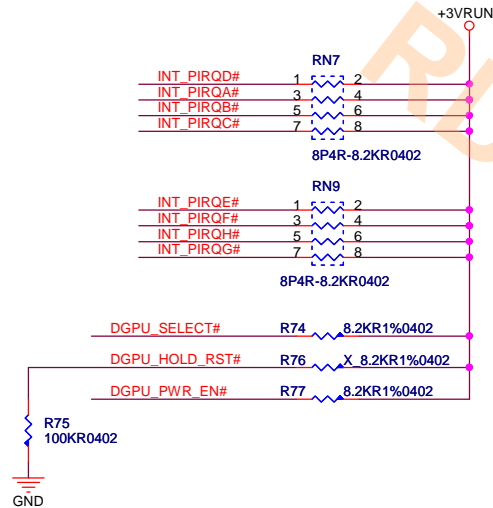


APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

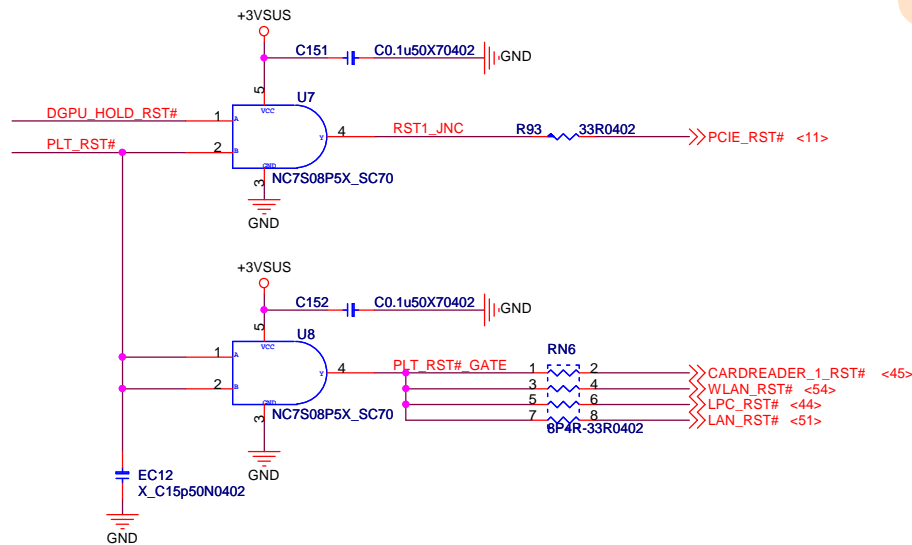
GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

Lynx Point (PCI,DDI)



DDI-B : DP
DDI-C : HDMI



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

Pin Configuration Table:

Pin	Function	Connection
AT8	BMBUSY#/GPIO0	10KR1%0402
F13	TACH1/GPIO1	44> KBSMI# <<
A14	TACH2/GPIO6	44> KBSCI# >>
G15	TACH3/GPIO7	VIA_ICC_EN#
Y1	GPIO8	
K13	LAN_PHY_PWR_CTRL/GPIO12	
AB11	GPIO15	VIA_JTAG_SATA4GP
AN2	SATA4GP/GPIO16	U_PWRGD >>
C14	TACH0/GPIO17	10KR1%0402
BB4	SCLOCK/GPIO22	BIOS_REC
Y10	GPIO24	VIA_HOST_ALERT#2
R11	GPIO27	10KR1%0402
AD11	GPIO28	DSW_WEAK_UP_EVENT
AN6	GPIO34	VIA_STP_PCI#
AP1	GPIO35/NMI#	VIA_EDID_SELECT#
AT3	SATA2GP/GPIO36	VIA_PCH_GPIO36
AK1	SATA3GP/GPIO37	VIA_PCH_GPIO37
AT7	SLOAD/GPIO38	10KR1%0402
AM3	SDATAOUT0/GPIO39	VIA_CRB_SV_DET
AN4	SDATAOUT1/GPIO48	10KR1%0402
AK3	SATA5GP/GPIO49	VIA_GPIO49
U12	GPIO57	X 10KR1%0402
C16	TACH4/GPIO68	
D13	TACH5/GPIO69	
G13	TACH6/GPIO70	
H15	TACH7/GPIO71	
BE41	VSS	
BE5	VSS	
C45	VSS	
A5	VSS	

GPIO Setting Table:

GPIO28	Setting
Internal pull up	Disable
Low	Disable

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

PCH_THRMTrip#_R

EC9
X_C15p50N0402

GND

Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug tran

USB 2.0

USB 2.0	USB 3.0
0	1
1	2
2	
3	
4	
5	
6	
7	
8	3
9	
10	
11	
12	
13	

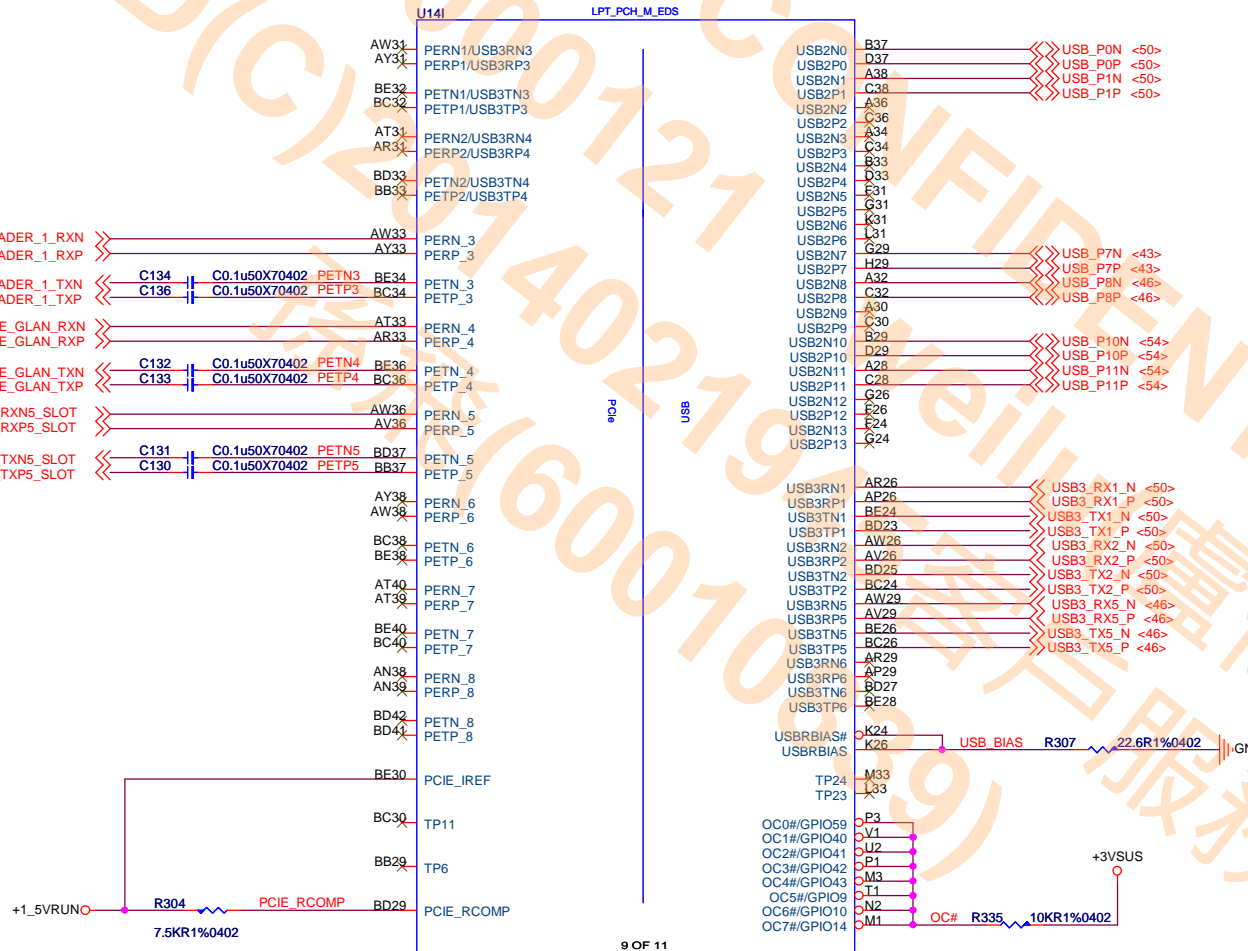
HM86 沒USB

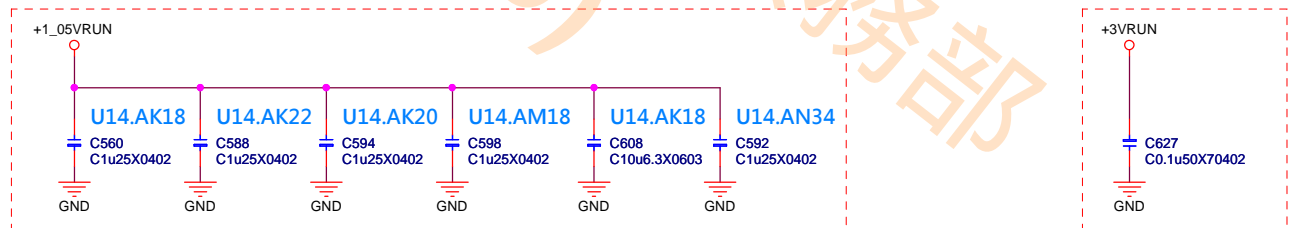
9 OF 11

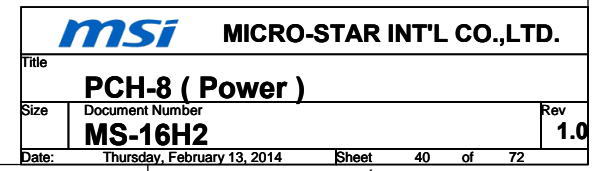
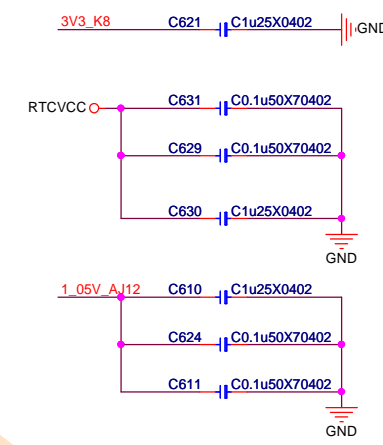
Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H2A
1	2	USB 3.0 Port 2	16H2A
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	16H21
9			NC
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

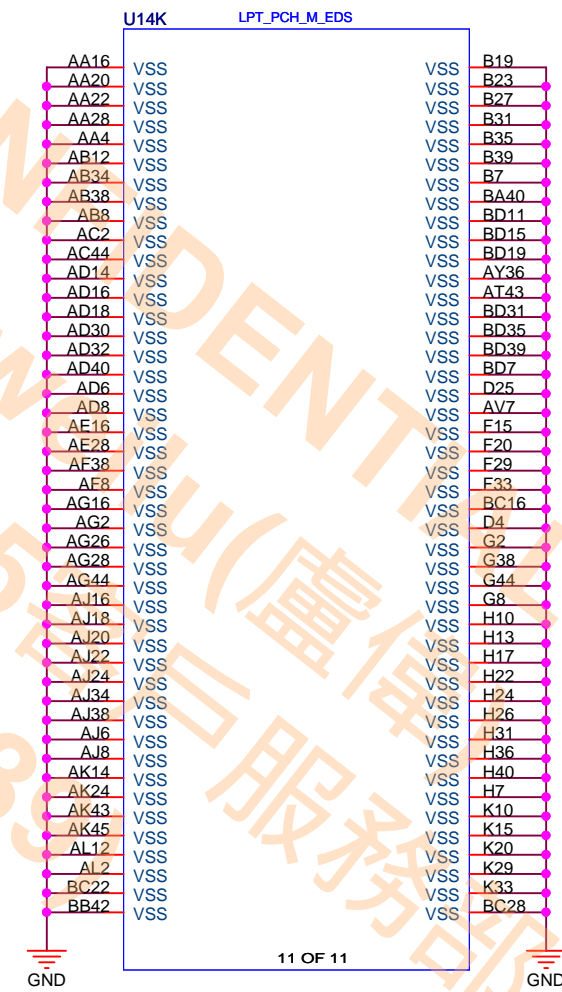
HM86 沒USB3.0 PORT 5,6



[illegible]

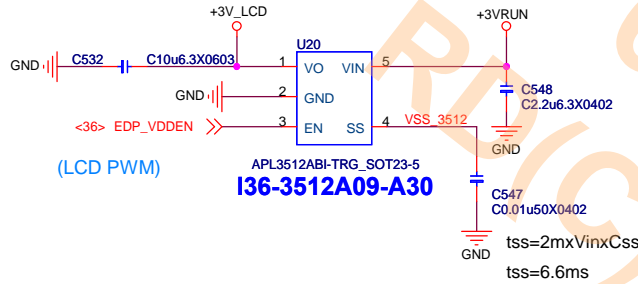
[illegible]

Lynx Point (GND)

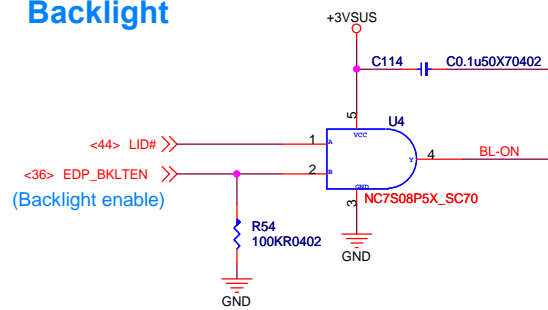


eDP Connector

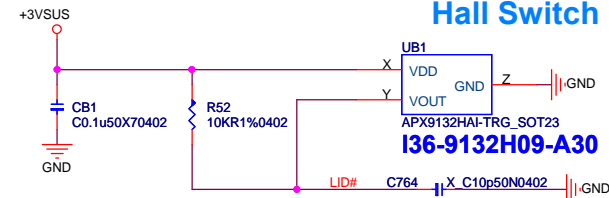
Pannel Device Logic Power



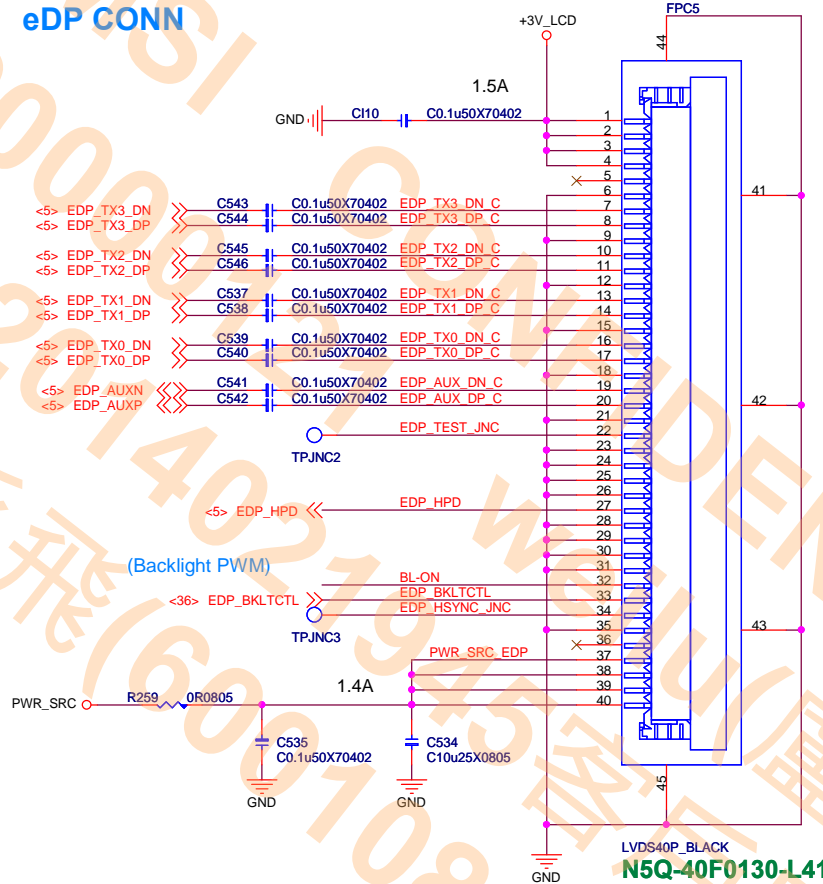
Backlight



Hall Switch



eDP CONN

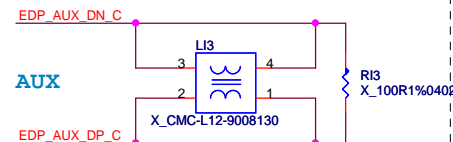
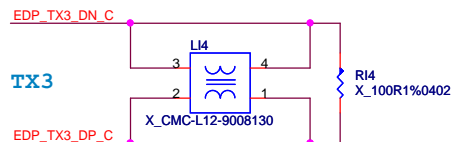
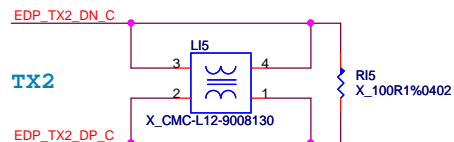
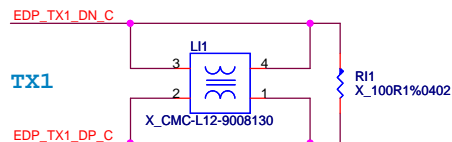
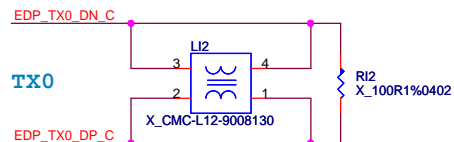


LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

Place Close eDP Connector

Reserve for EMI

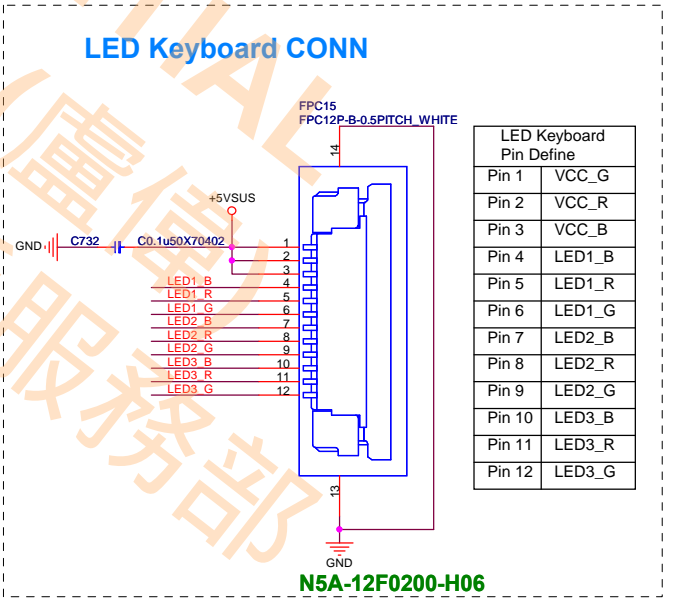
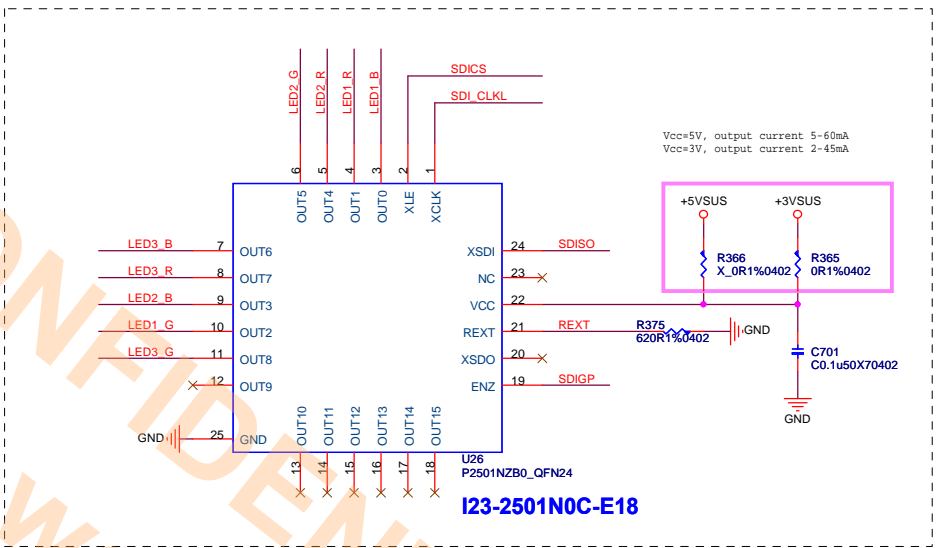
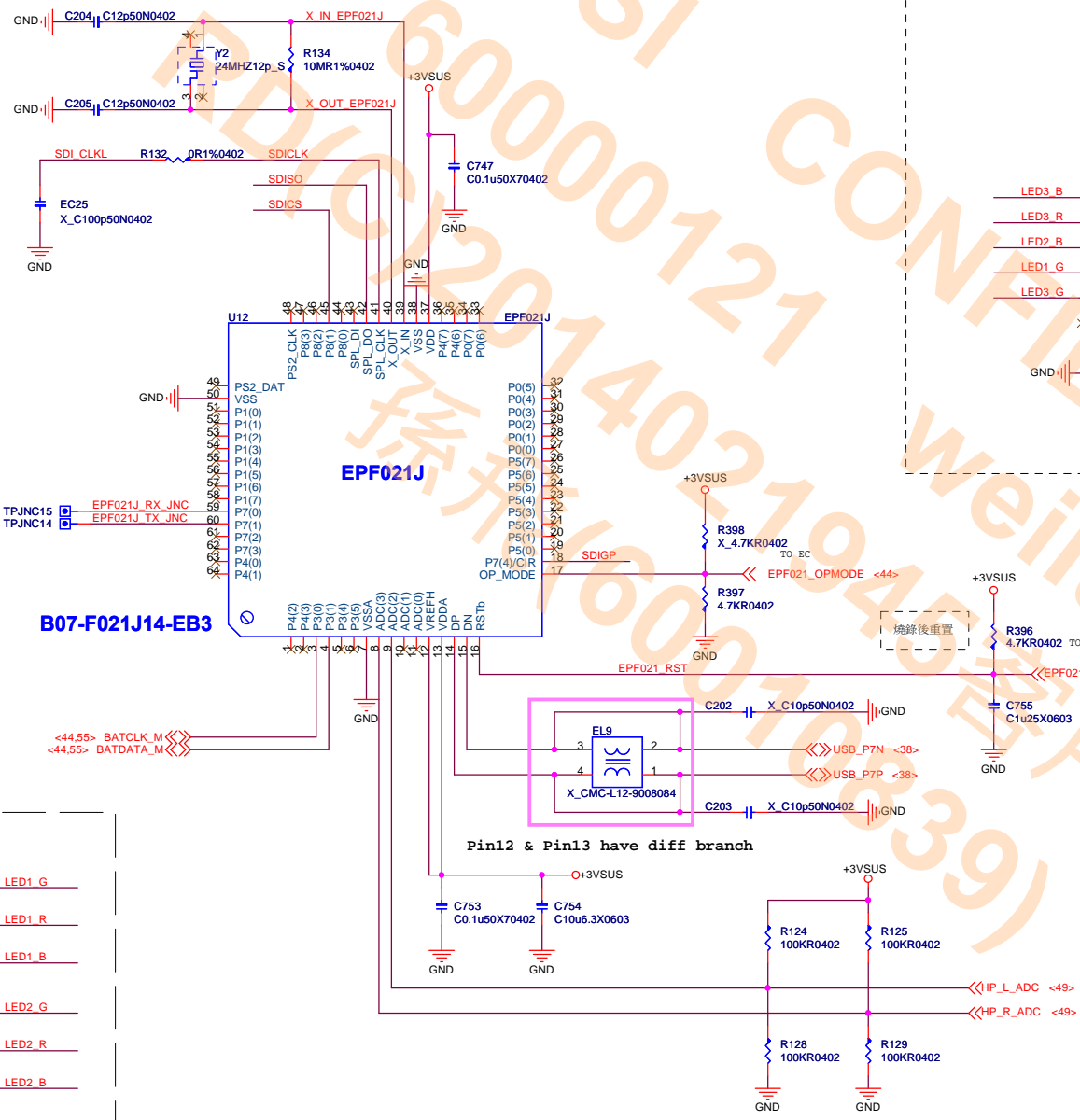


msi

MICRO-STAR INT'L CO.,LTD.

Title		eDP Connector	
Size	Document Number	Rev	
	MS-16H2	1.0	
Date:	Friday, January 03, 2014	Sheet	42 of 72

LED 8051 Controller



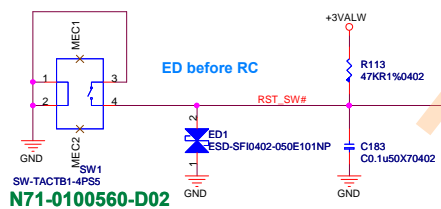
EMI

GND	C725	X	C100p50N0402	LED1_G
GND	C713	X	C100p50N0402	LED1_R
GND	C709	X	C100p50N0402	LED1_B
GND	C728	X	C100p50N0402	LED2_G
GND	C727	X	C100p50N0402	LED2_R
GND	C726	X	C100p50N0402	LED2_B
GND	C731	X	C100p50N0402	LED3_G
GND	C730	X	C100p50N0402	LED3_R
GND	C729	X	C100p50N0402	LED3_B

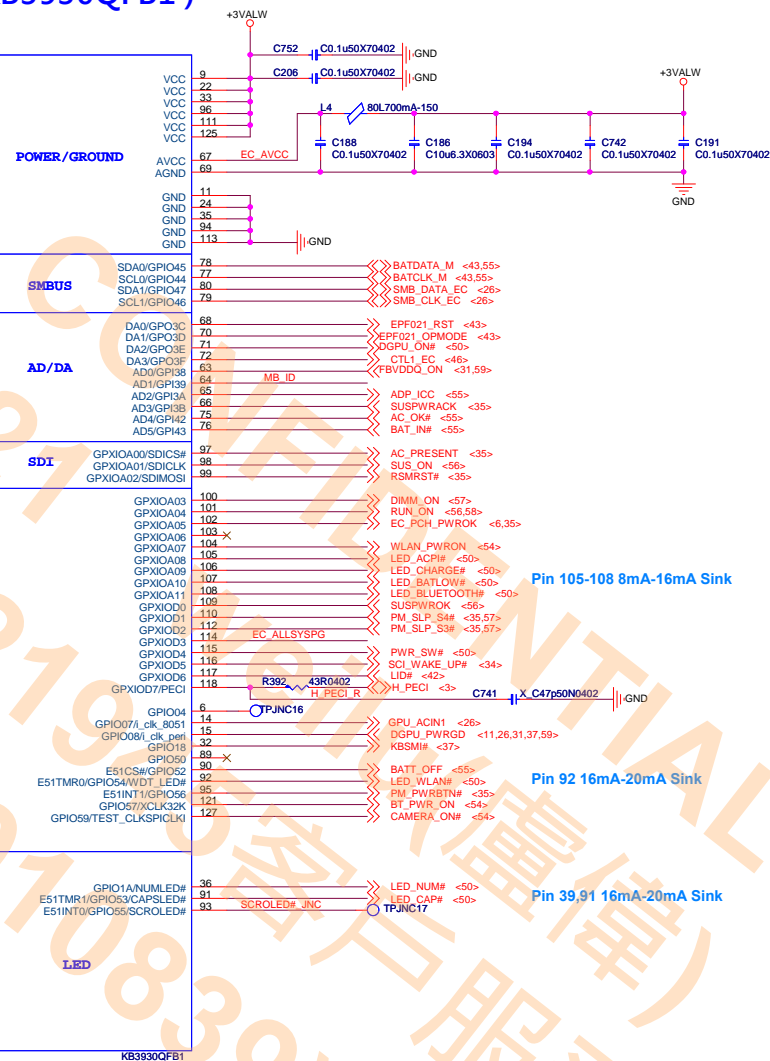
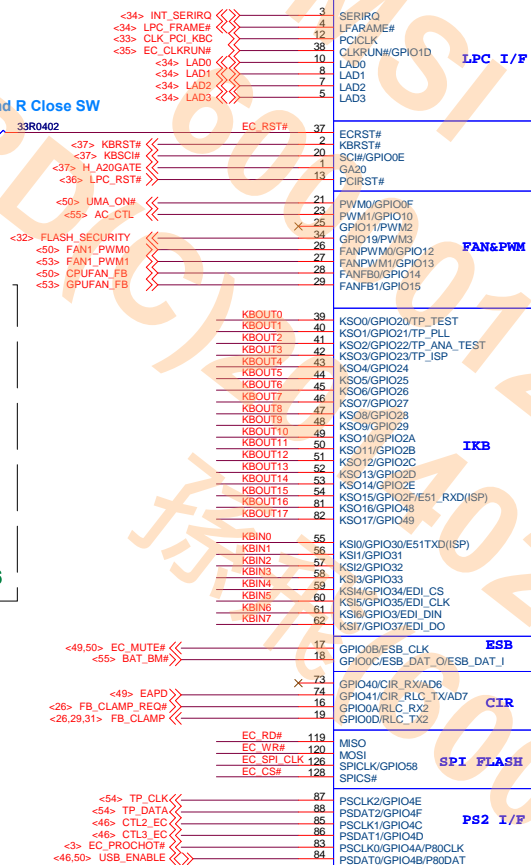
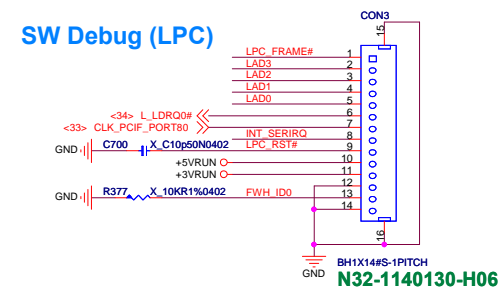
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC(KB3930QFB1)

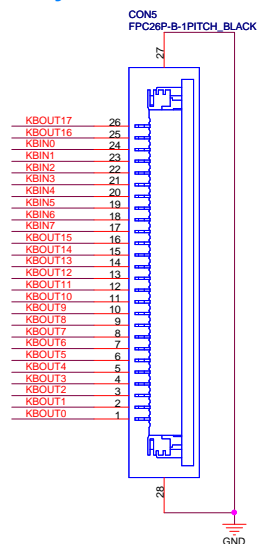
Hardware Reset



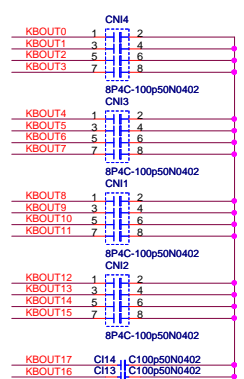
SW Debug (LPC)



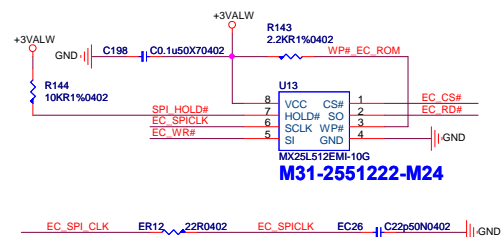
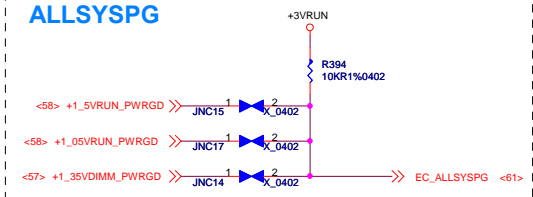
Keyboard conn



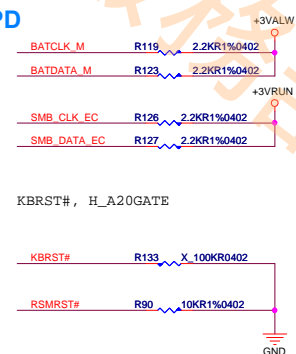
N5A-26F0340-H06



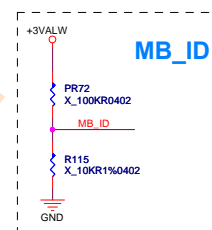
ROM

**ALLSYSPG**

PU/PD



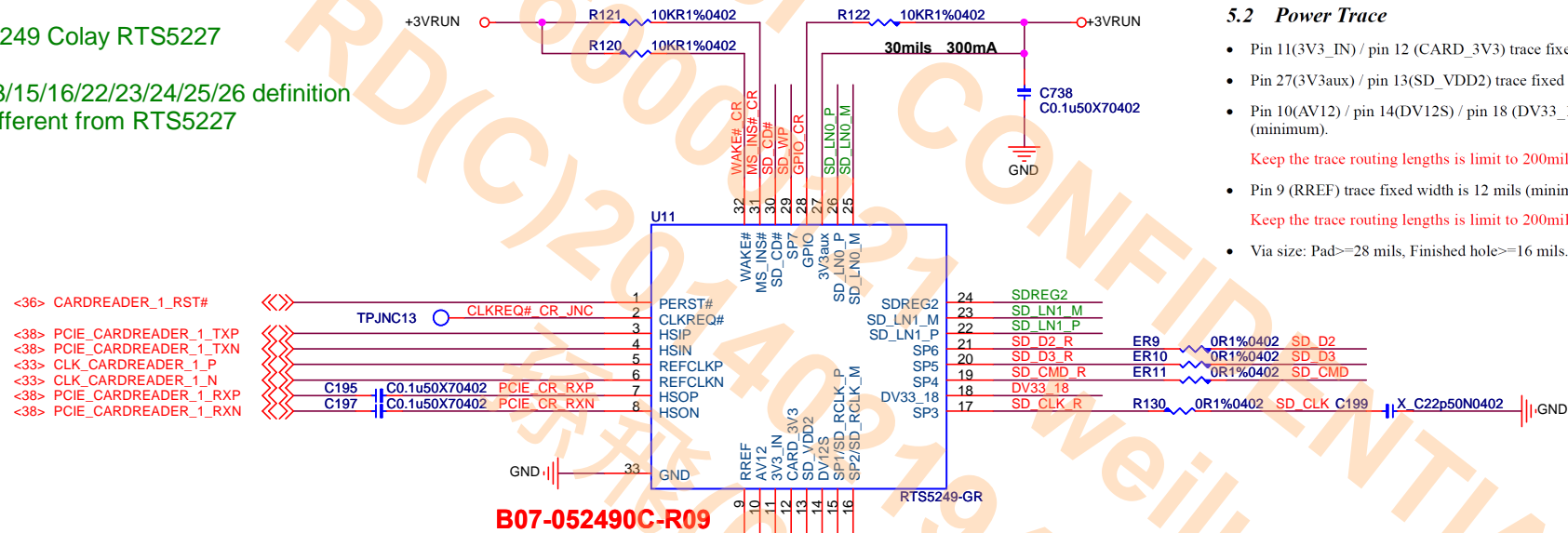
MB_ID



CardReader (RTS5249)

RTS5249 Colay RTS5227

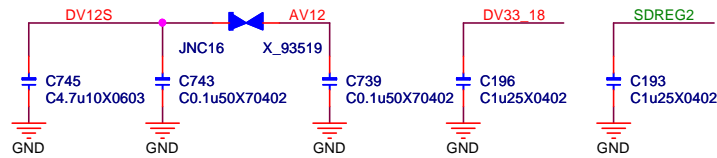
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



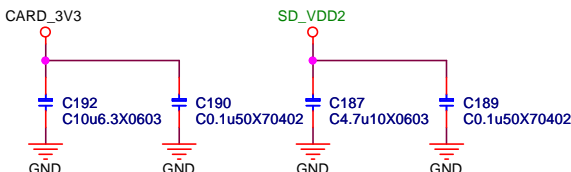
5.2 Power Trace

- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.

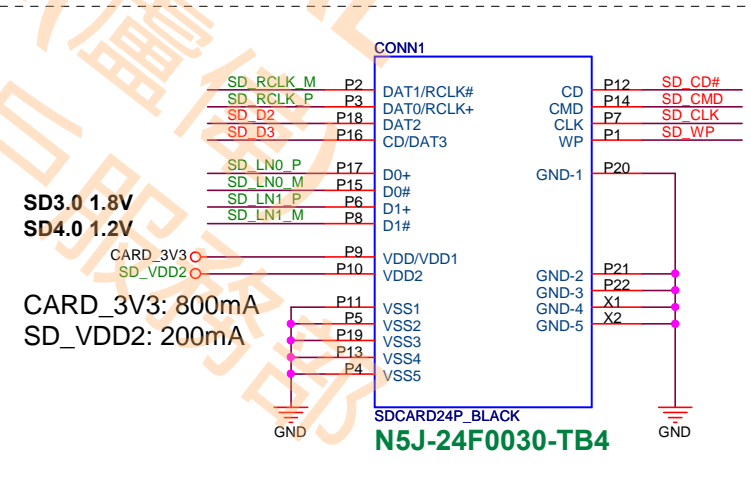
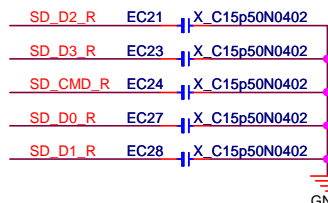
Close Chip



Close Connector

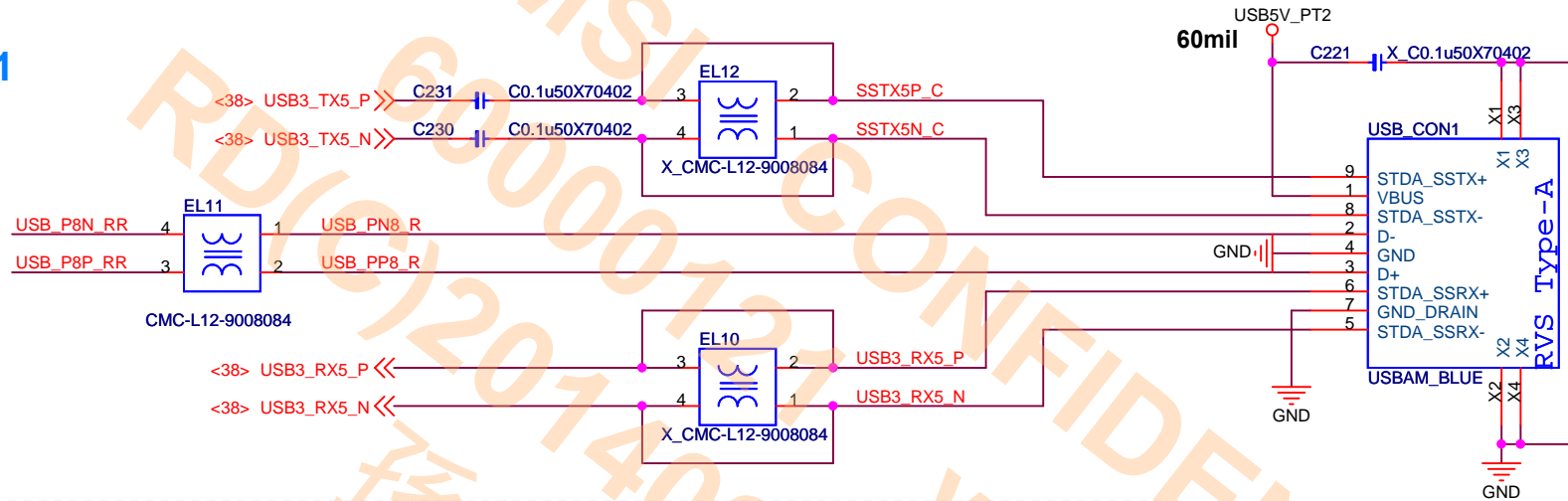


EMI



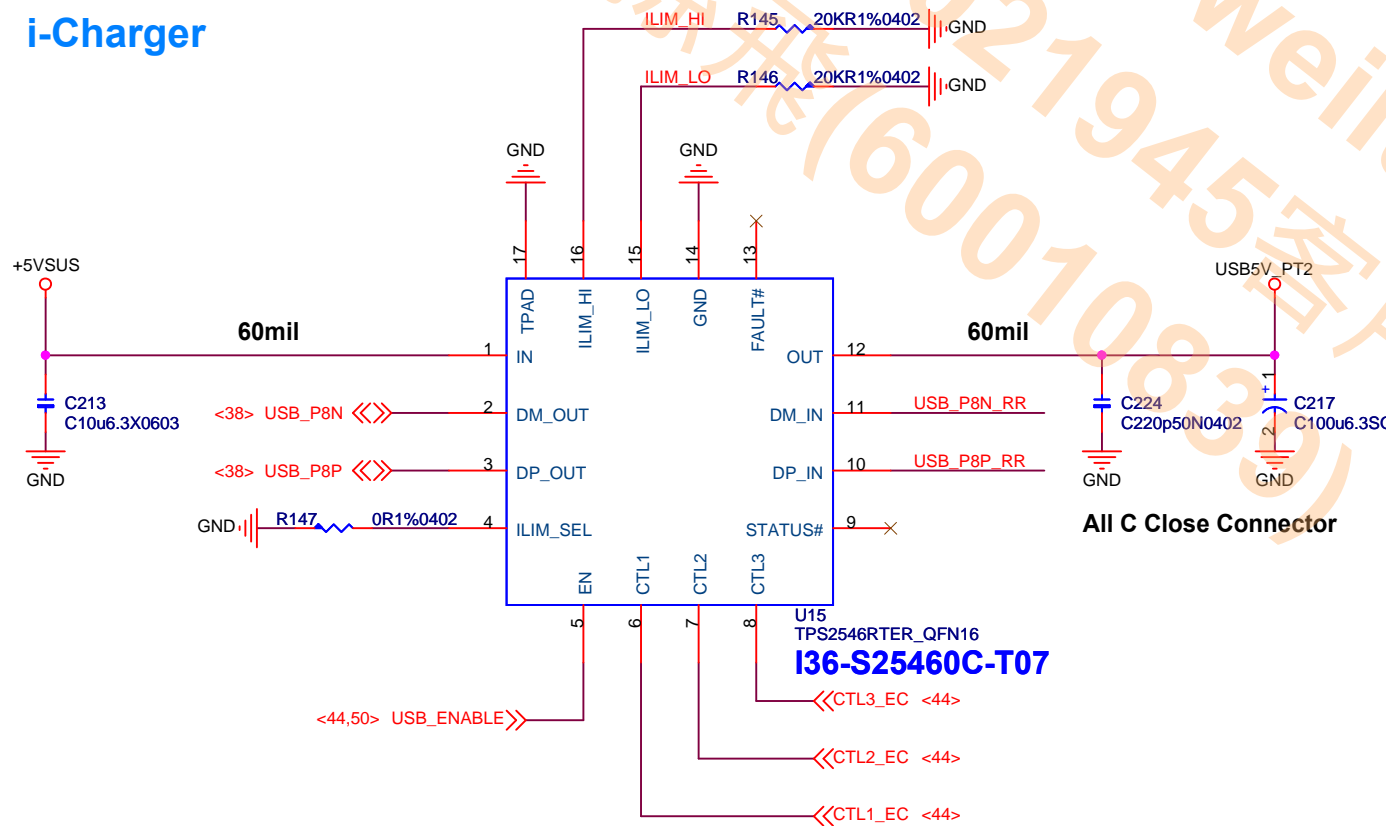
USB3.0 CNT-1

USB3.0 Port-6
USB2.0 Port-9



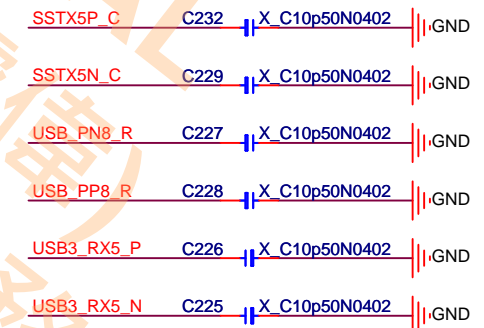
N53-09M0241-AF2

i-Charger



All C Close Connector

EMI

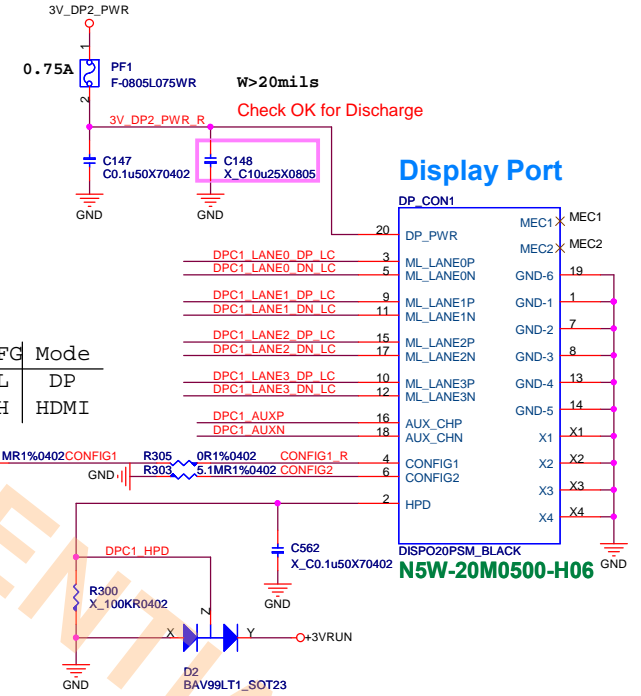
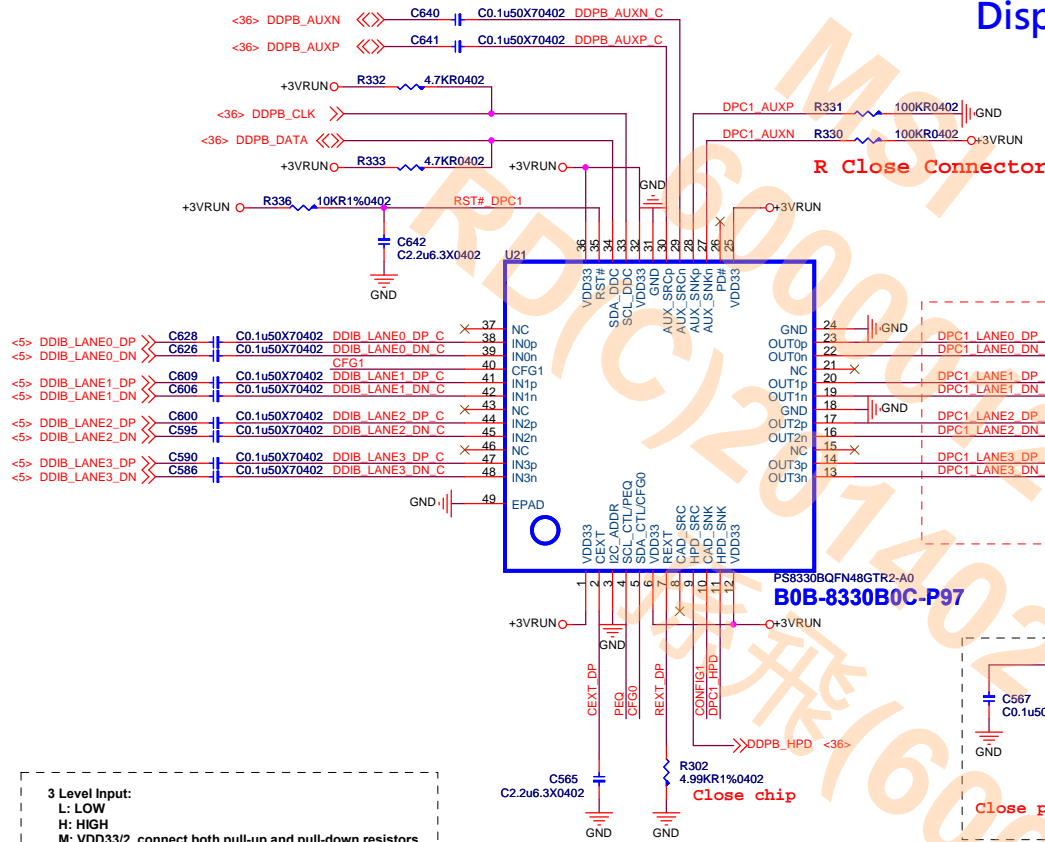


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Title			USB 3.0 / iCharger	
Size	Document Number		Rev	
	MS-16H2		1.0	
Date:	Friday, January 03, 2014		Sheet	46 of 72

Display Port



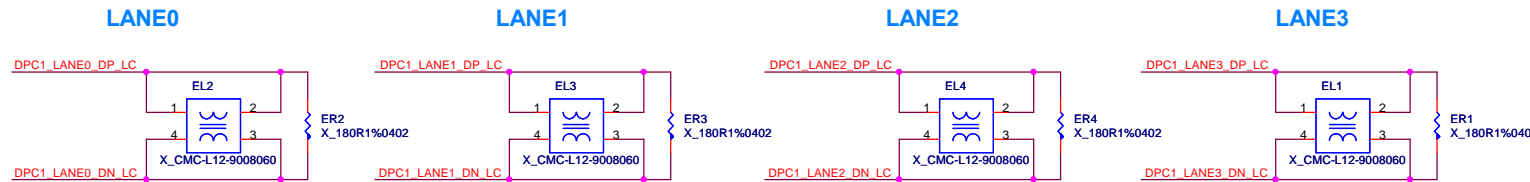
CAD_SNK Have internal Pull down 1Mohm.
 HPD_SNK Have internal Pull down 150kohm.
 No problem with Leakage from DP device
 The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
 L: default, automatic EQ enable & AUX interception enable
 H: automatic EQ disable & AUX interception enable
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

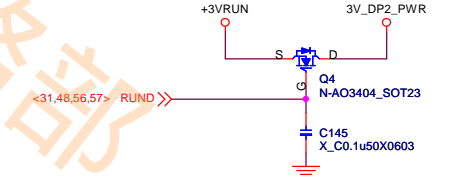
Configuration pin for auto test and input offset cancellation, 3.3V I/O, internal pull up at ~150K Ohm
 L: default, auto test disable & input offset cancellation enable
 H: auto test enable & input offset cancellation enable
 M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 H: HEQ, compensate channel loss up to 15dB @ HBR2
 M: LLEQ, compensate channel loss up to 5dB @ HBR2

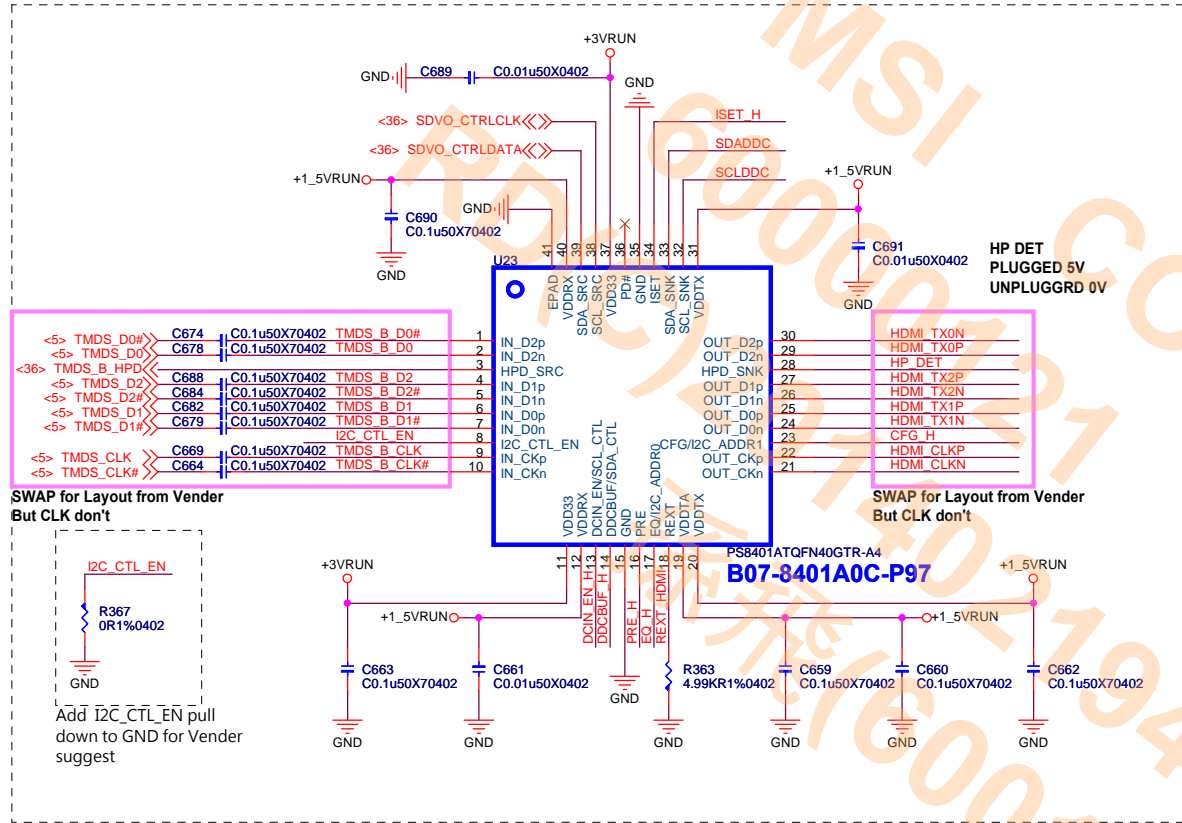
EMI Close Connector



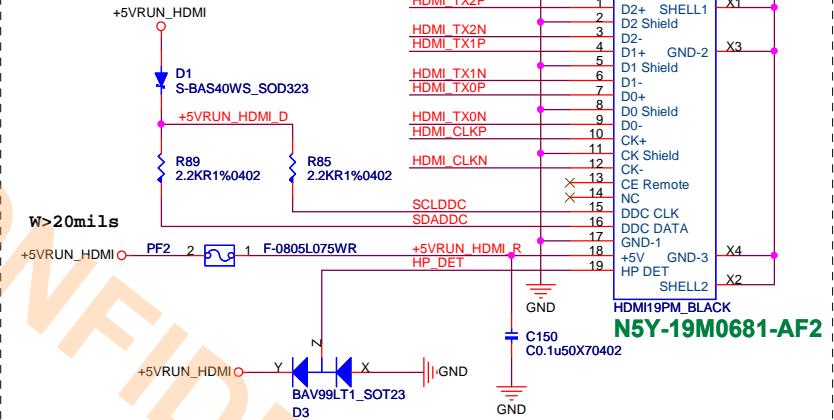
Avoid DP Leakage



HDMI Repeater



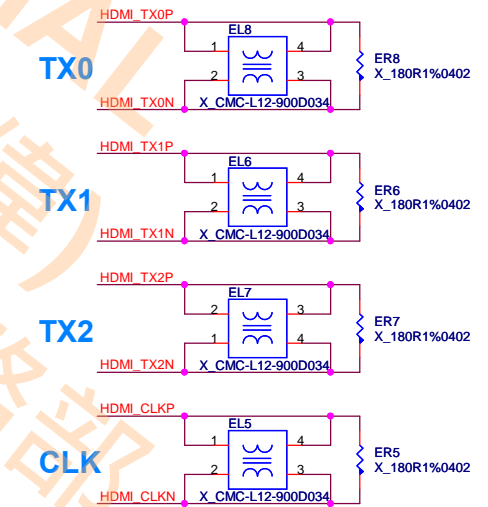
HDMI Connector



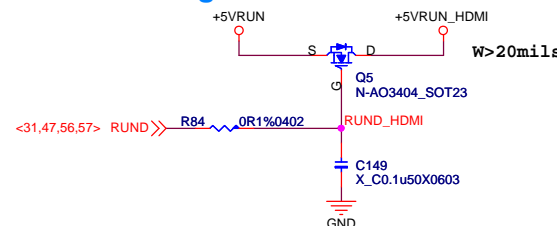
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector

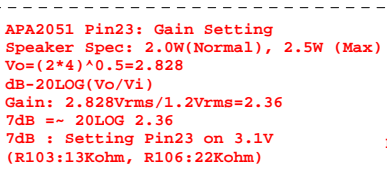
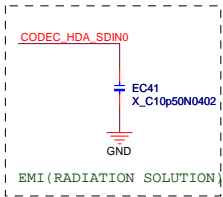
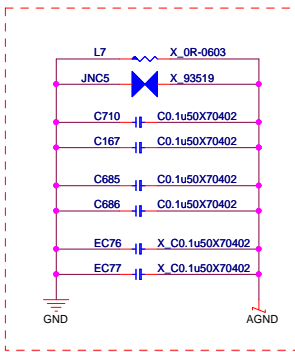


Avoid HDMI Leakage

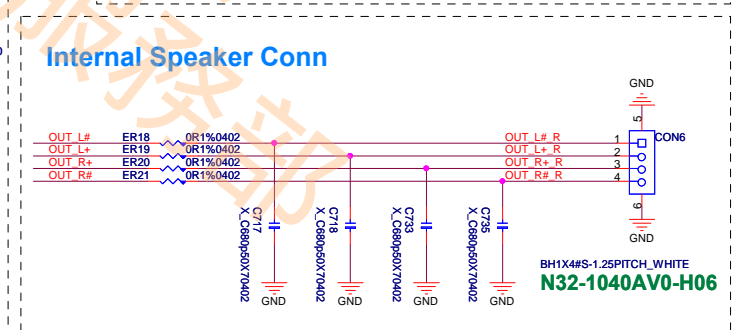
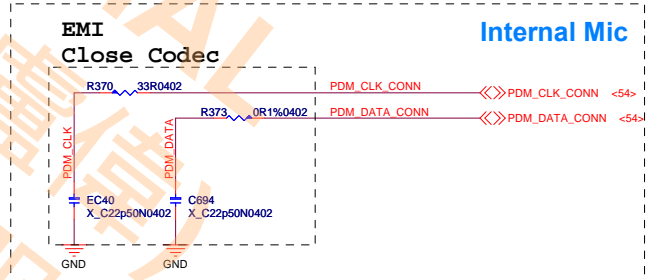
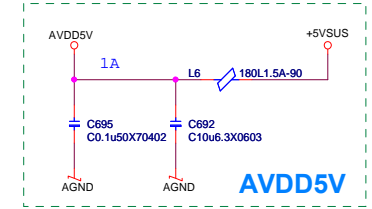
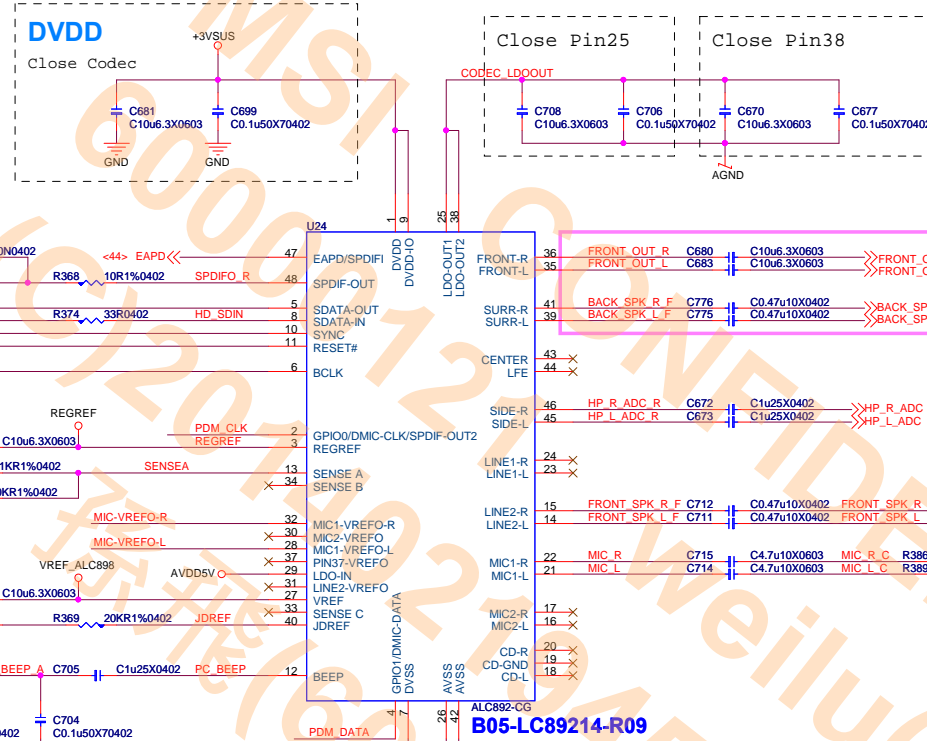
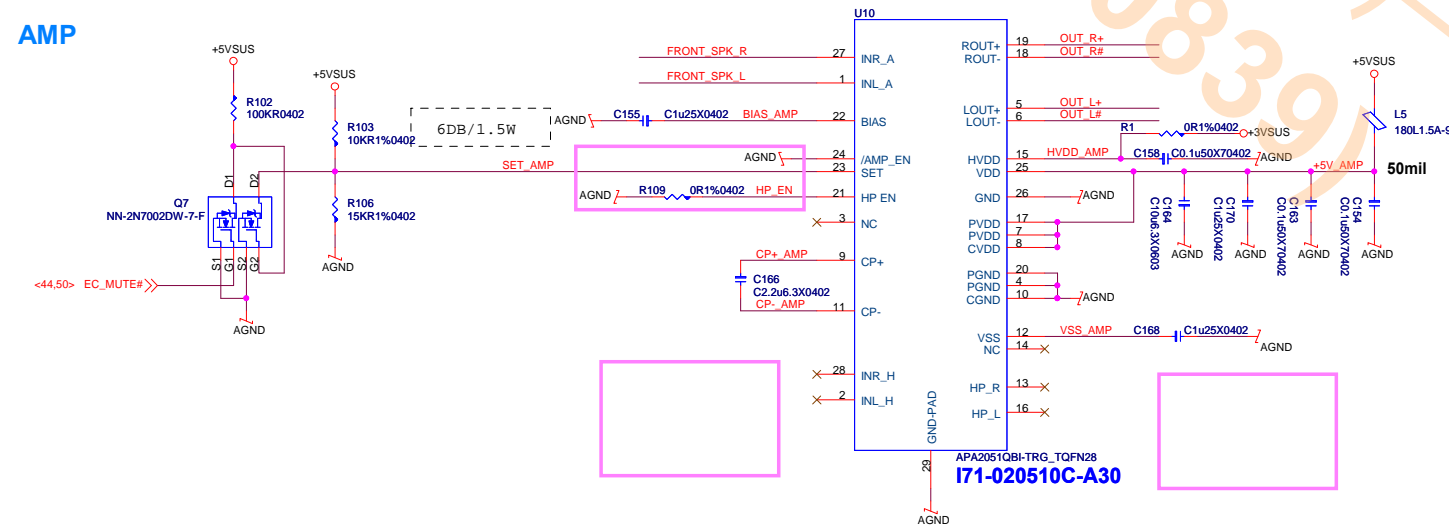


ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Audio CODEC/Audio AMP

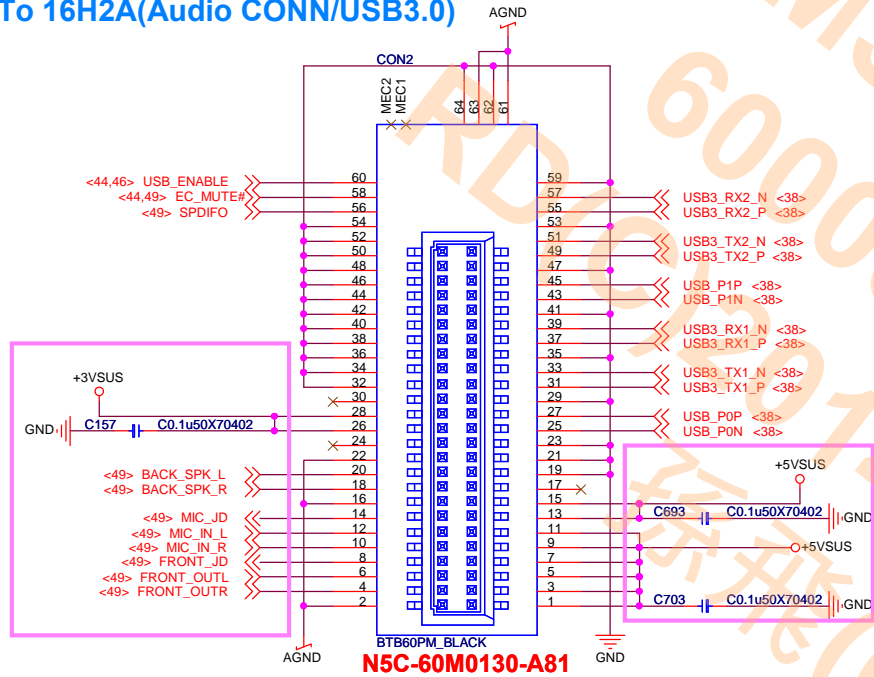


For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

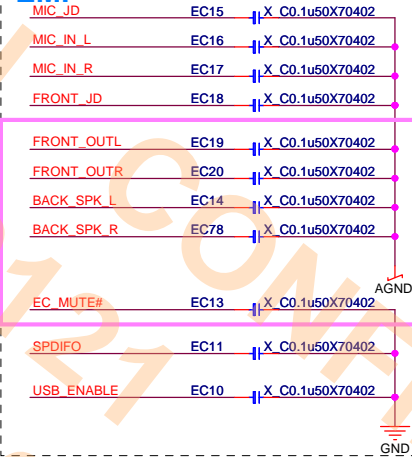


CPU FAN/BTB CONN

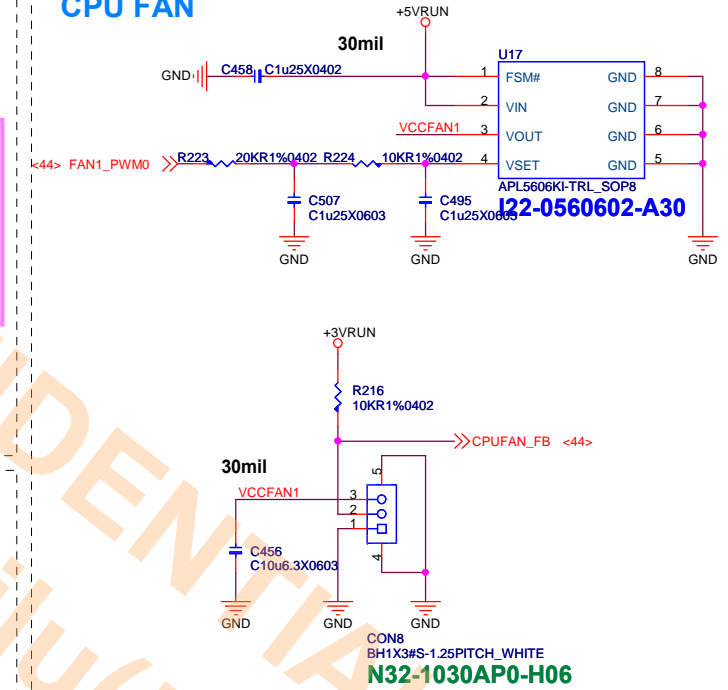
To 16H2A(Audio CONN/USB3.0)



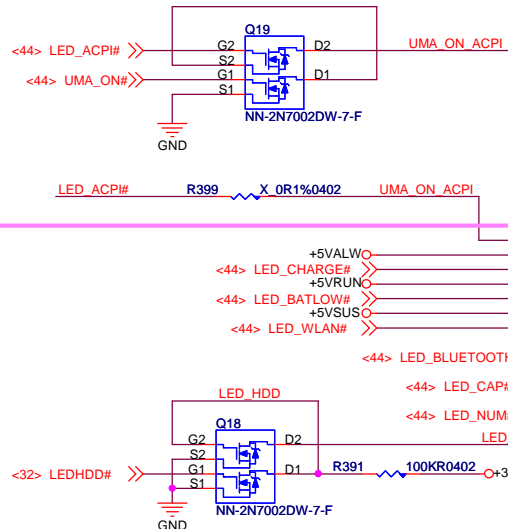
EMI



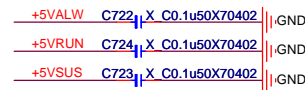
CPU FAN



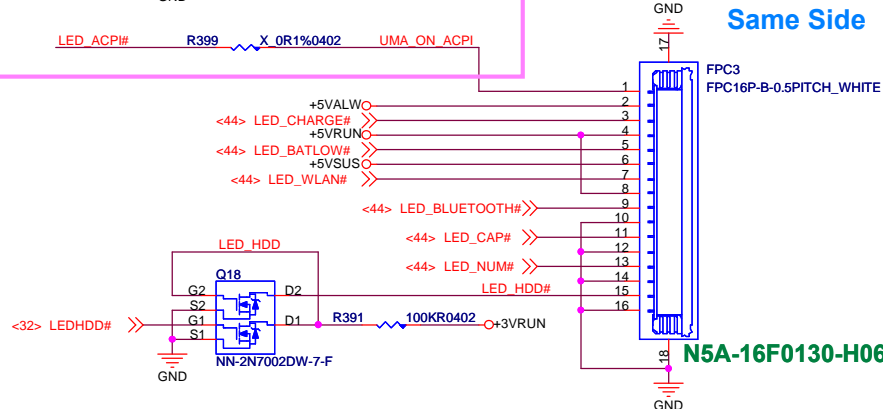
S3 Breath S0 No active



To 16H2B(LED Board)



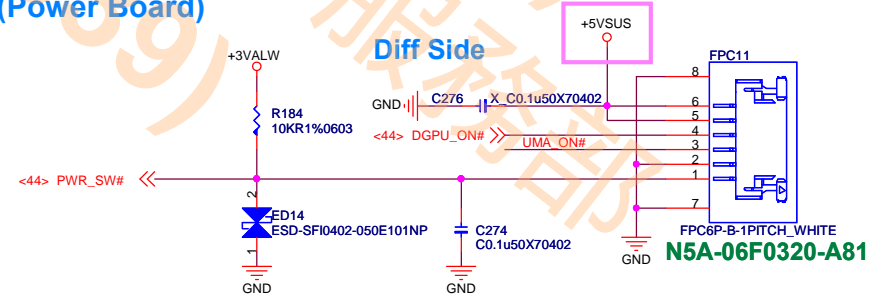
Same Side



EMI



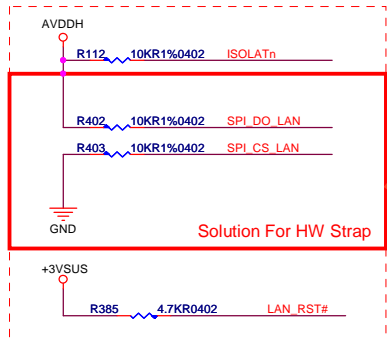
To 16H2C (Power Board)



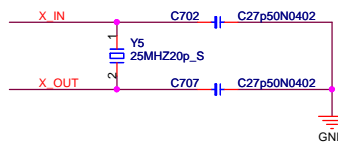
msi

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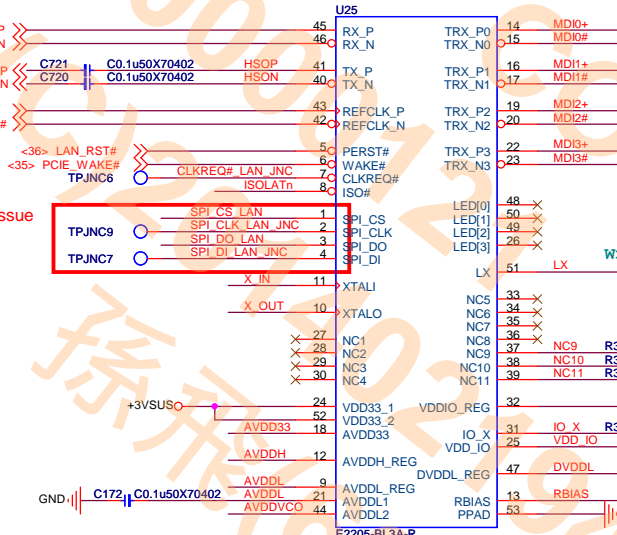
GIGA LAN(BigFoot BFN2205B)



RST# spacing 20mils

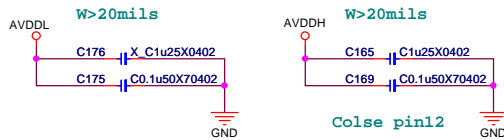


For LAN lost issue

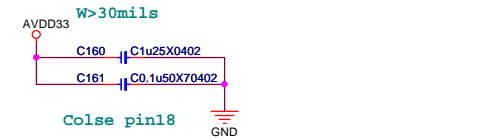


B06-E22050C-Q24

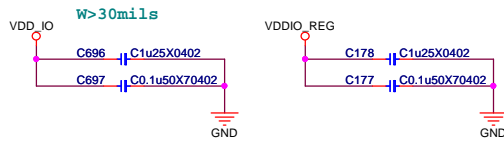
MAC 燒 CHIP
內,有次數限制



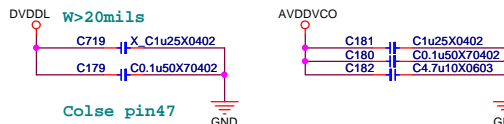
Colse pin1



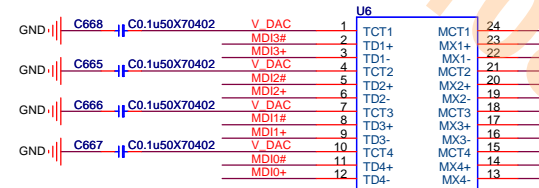
Colse pin18



VDDIO_REG

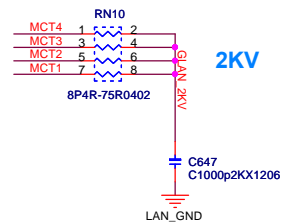


Colse pin4

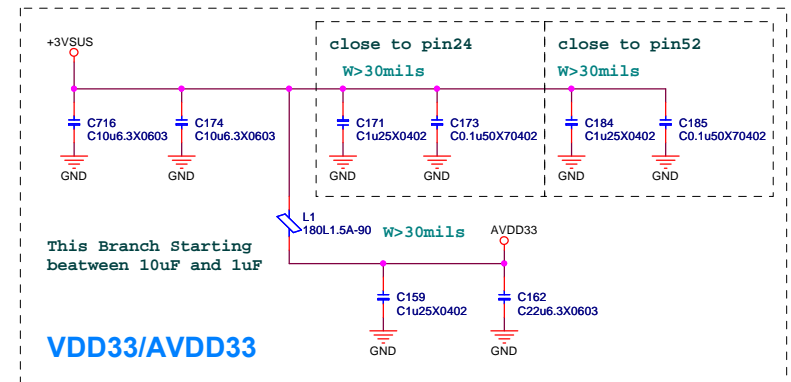
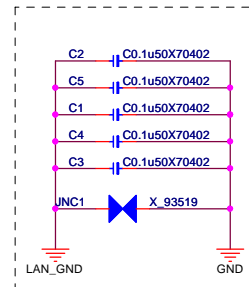


GST5009-VLF

L05-0200150-B09

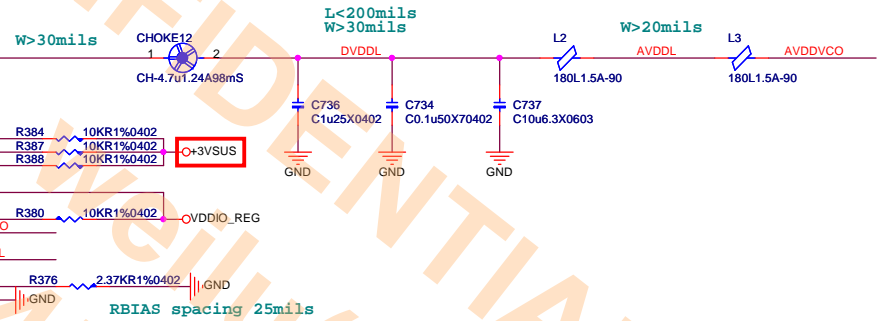


2KV



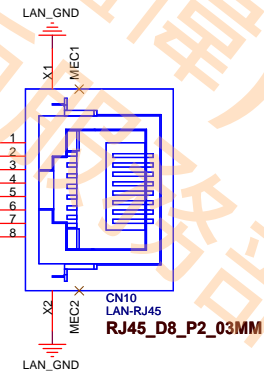
This Branch Starting
between 10uF and 1uF

VDD33/AVDD33



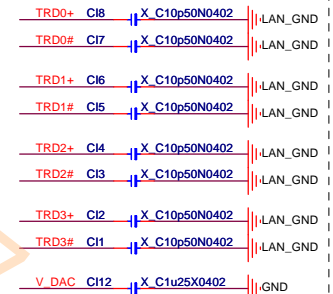
The diagram shows a red wire connecting a terminal labeled **+3VSUS** to a component labeled **KR1%0402**. Another component labeled **KR1%0402** is shown nearby.

RBIAS spacing 25mils



N55-08F0691-AF2

EMI



TRD3#

V_DAC

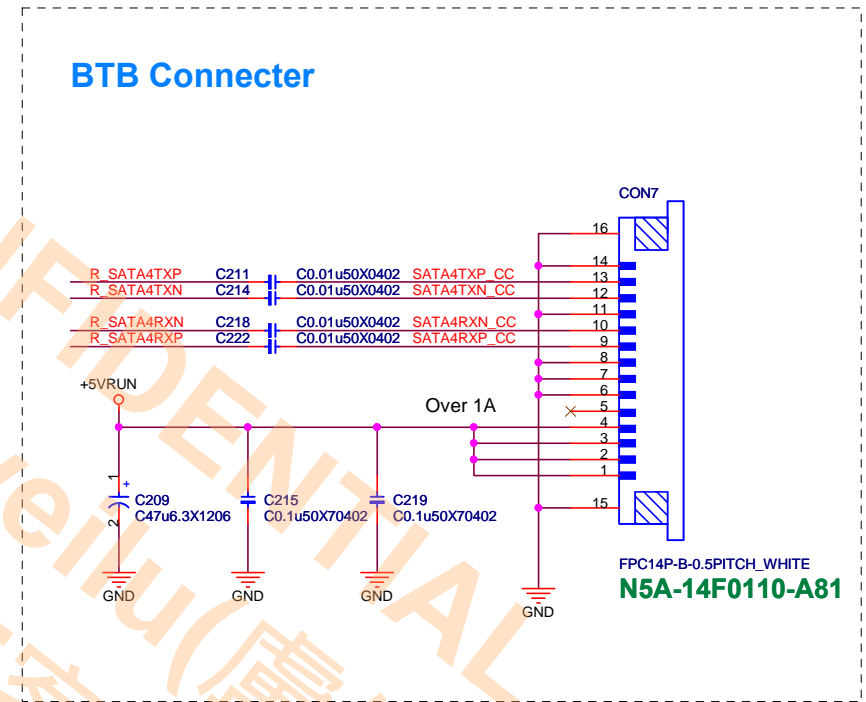
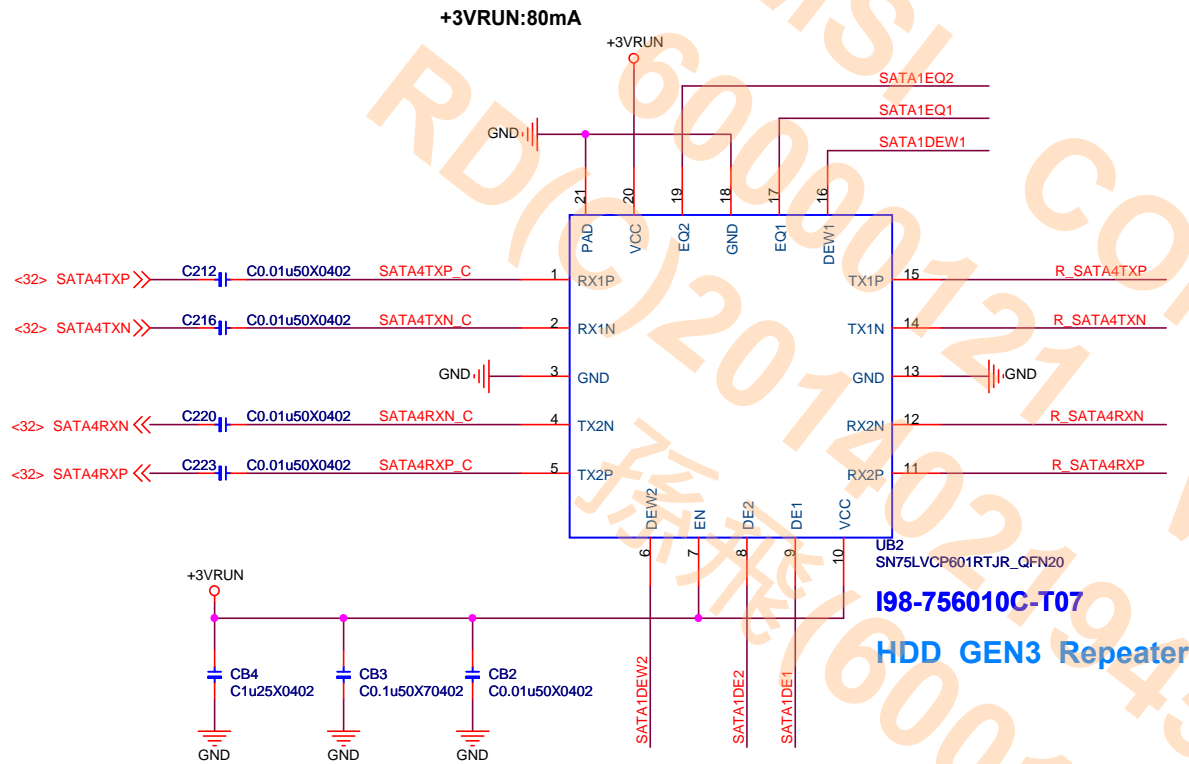
msi MICRO-STAR INT'L CO.,LTD.

Title **GIGA LAN(BigFoot BFN2205B)**

Size	Document Number	Rev
	MS-16H2	1.0

Date:	Friday, January 03, 2014	Sheet	51	of	72
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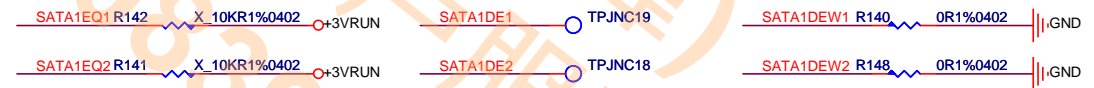
HDD (With Repeater)



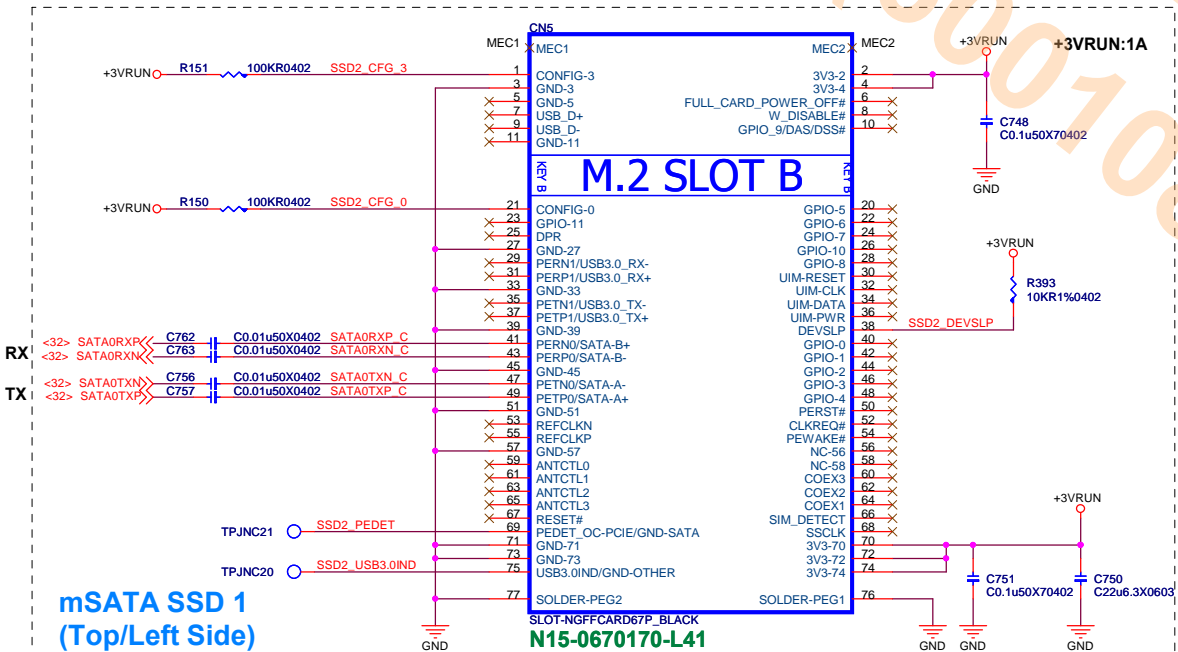
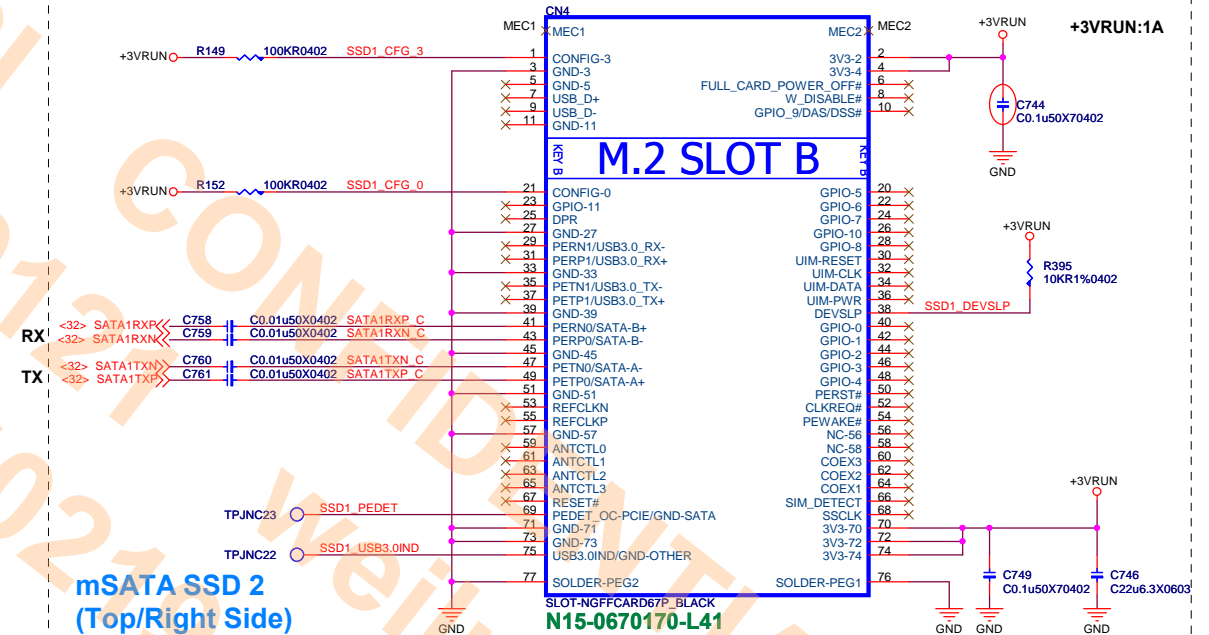
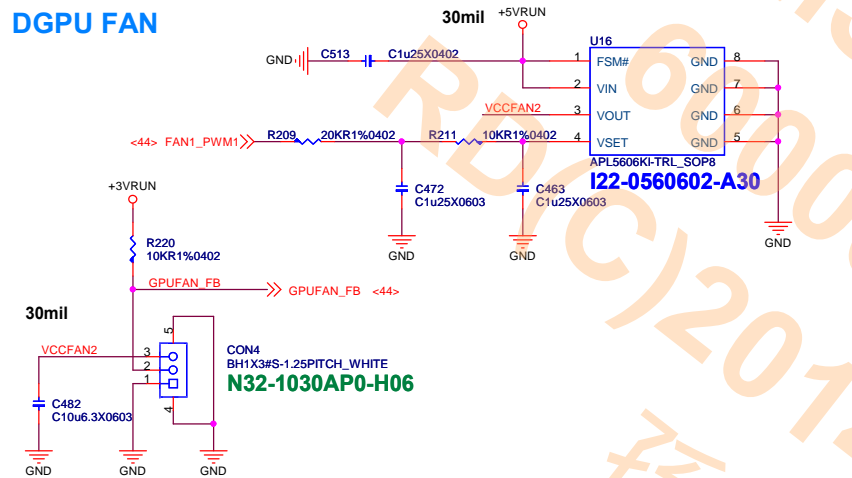
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (<i>default</i>)	−4	NC (<i>default</i>)	0
0	0	0	7
1	−2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (<i>default</i>)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)



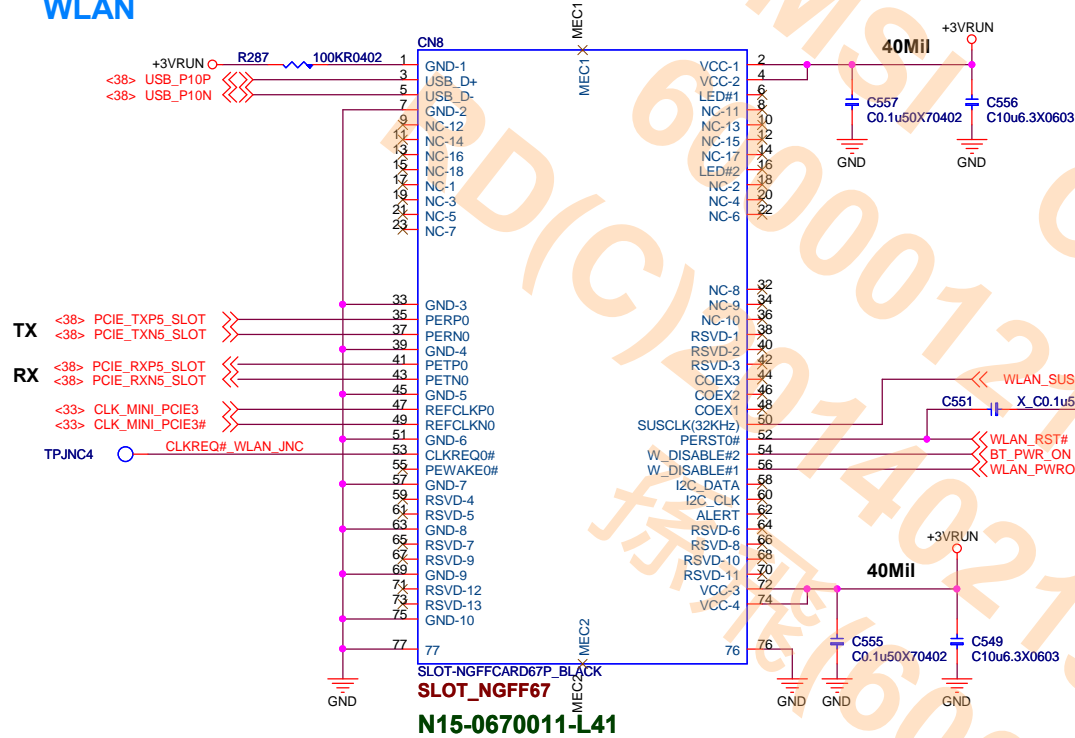
SSD/ DGPU FAN



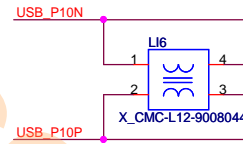
40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

WLAN /Camera/ClickPad/FP

WLAN

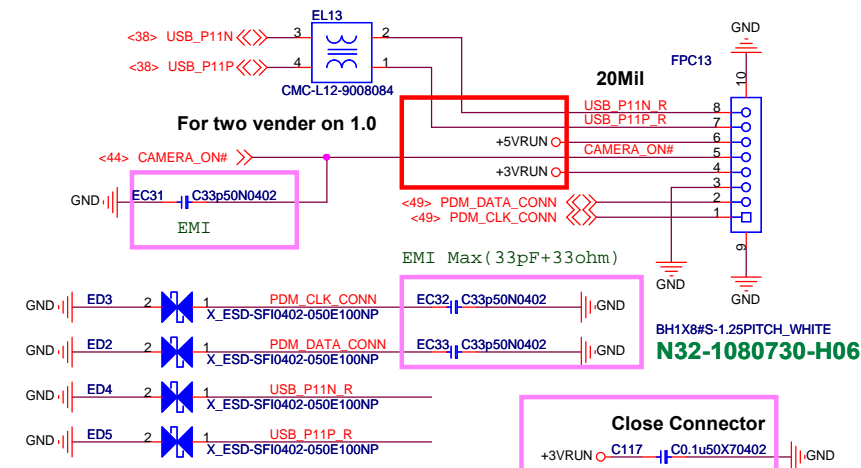


EMI

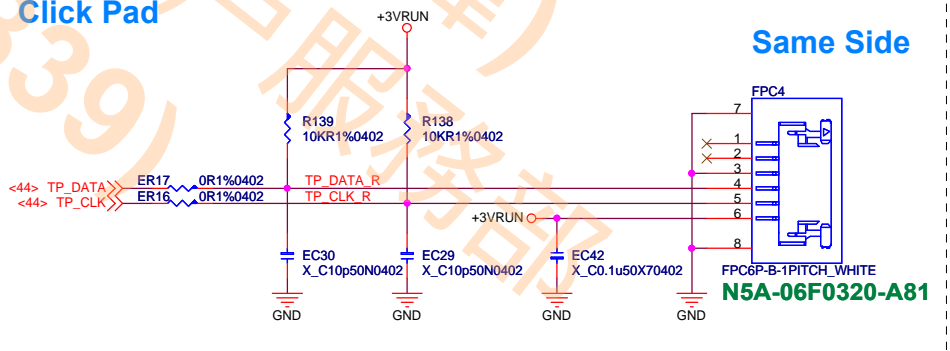


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

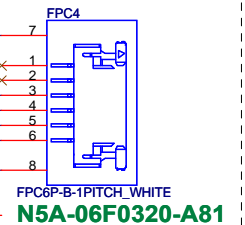
CAMERA



Click Pad



Same Side



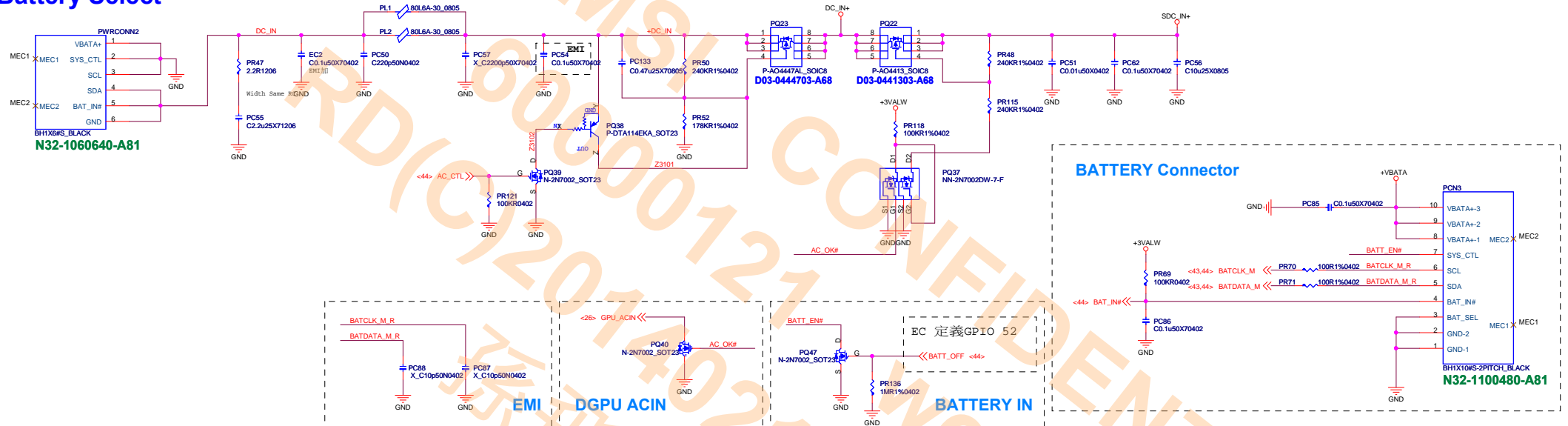
msi

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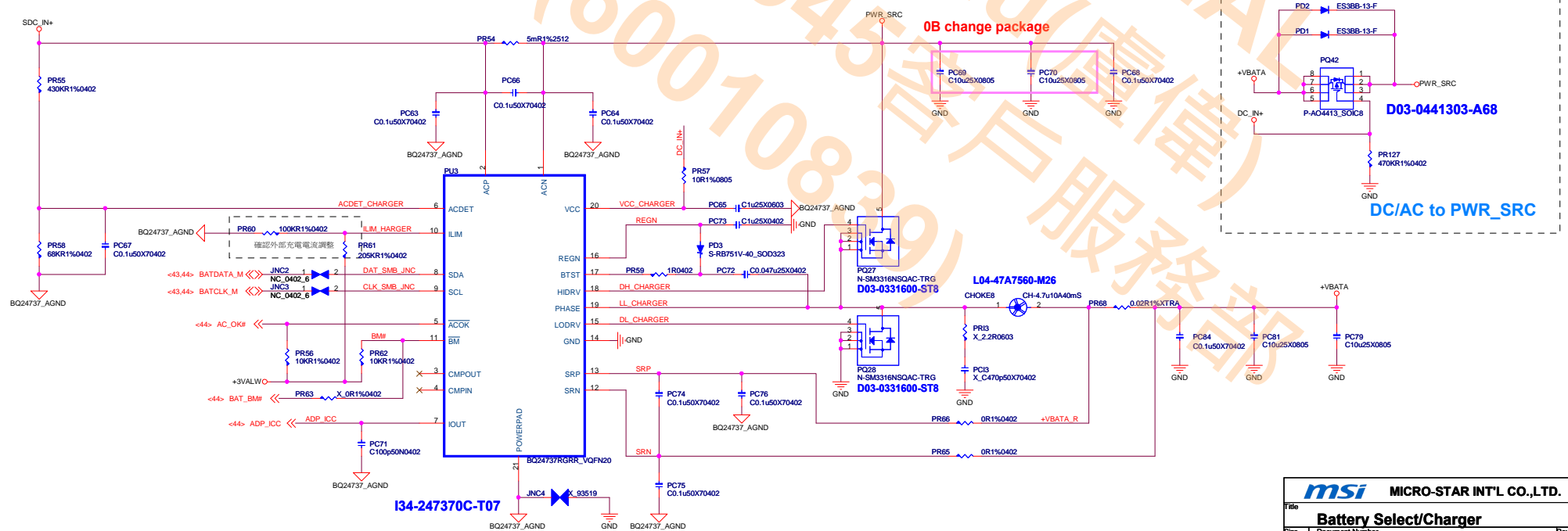
Title	WLAN /Camera/ClickPad/FP		
Size	Document Number	Rev	1.0
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Battery Select/Charger

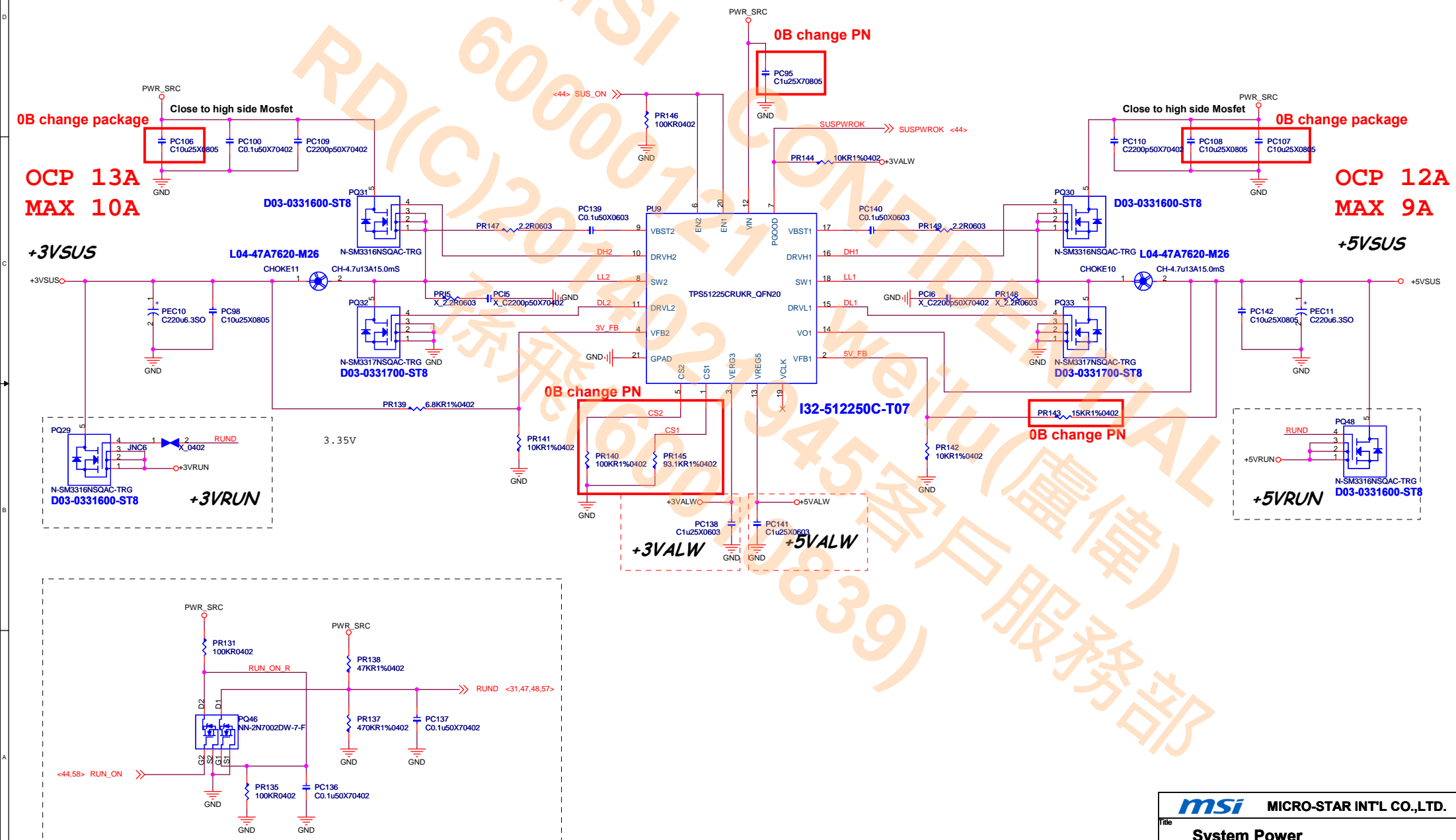
Battery Select



Battery Charger

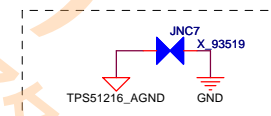
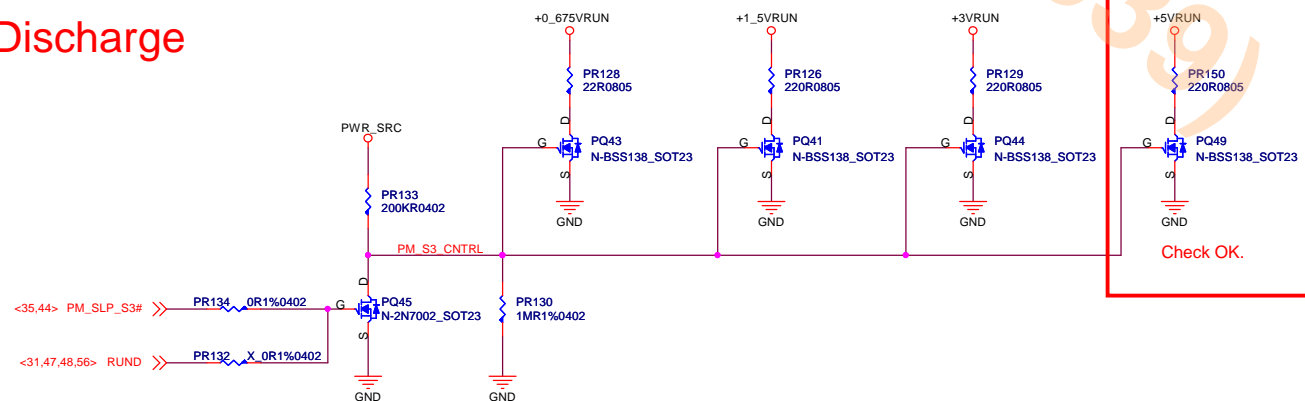
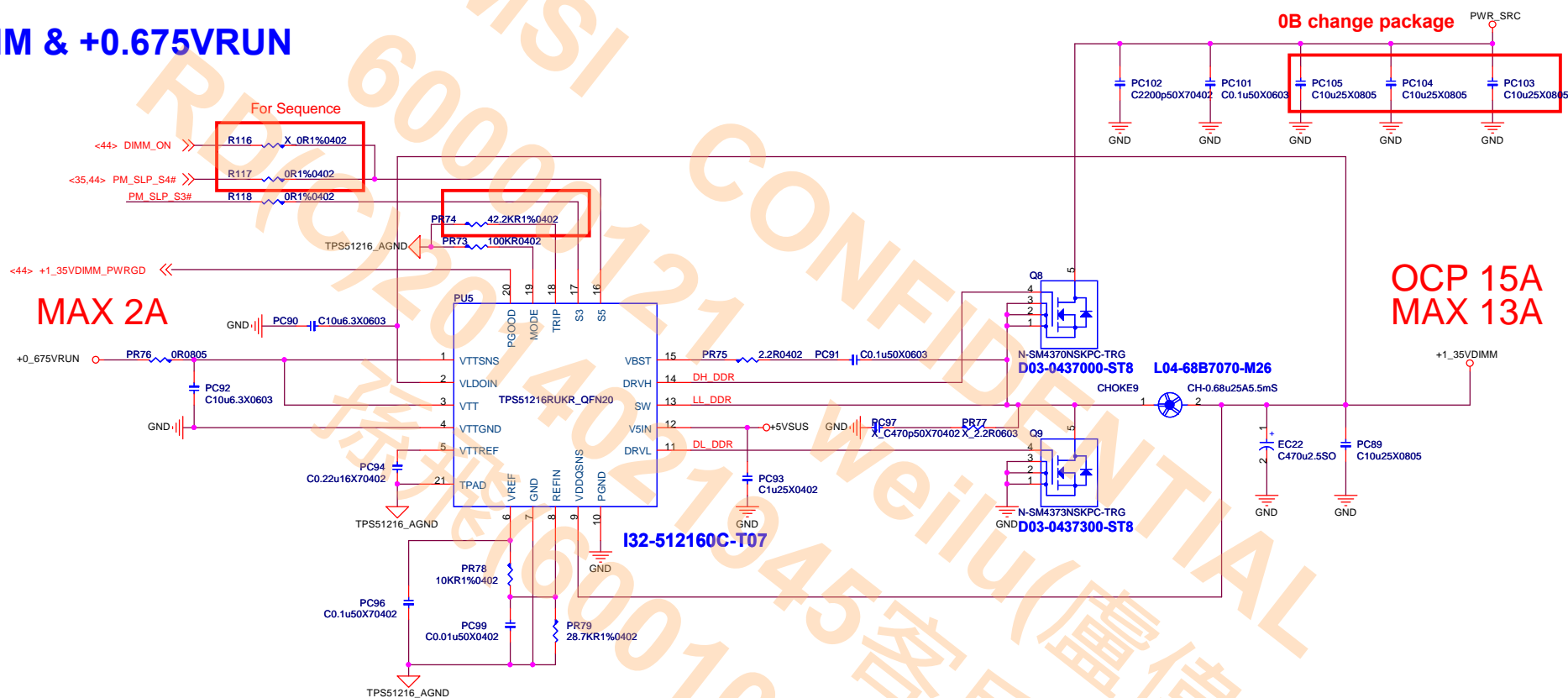


System Power



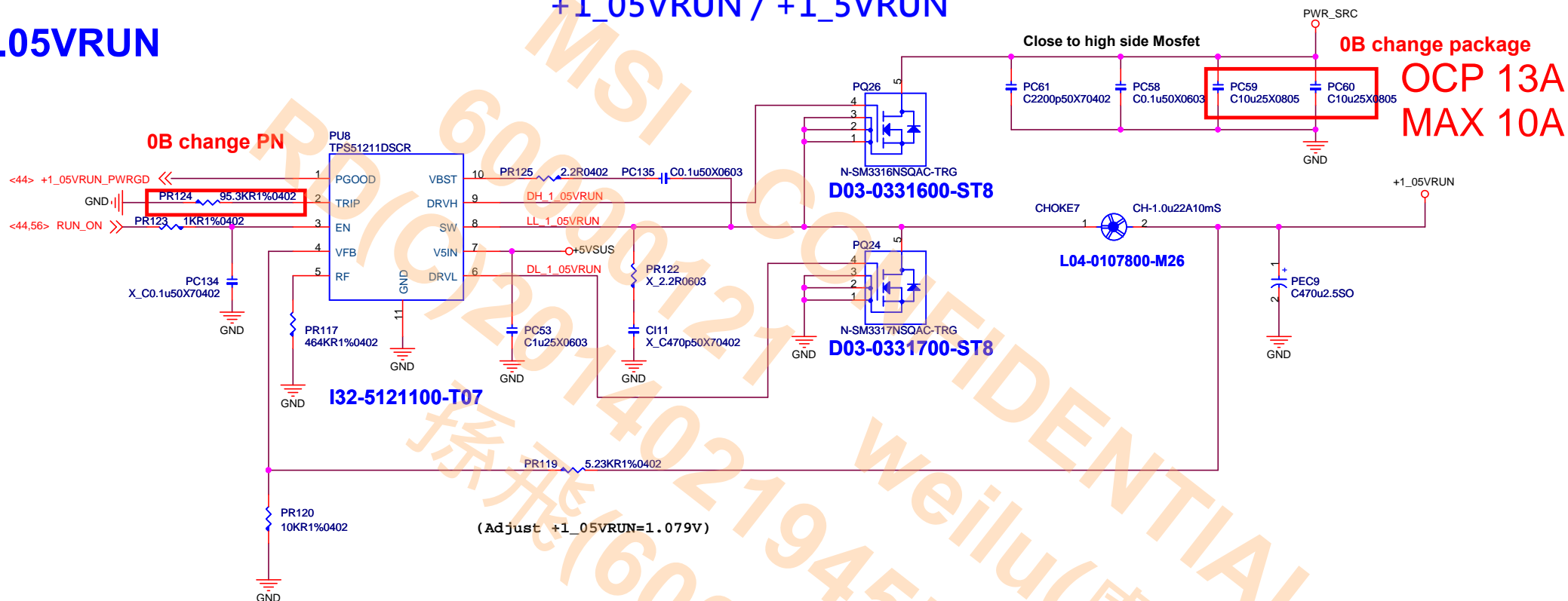
+1.35VDIMM & +0.675VRUN

+1.35VDIMM/+0.675VRUN

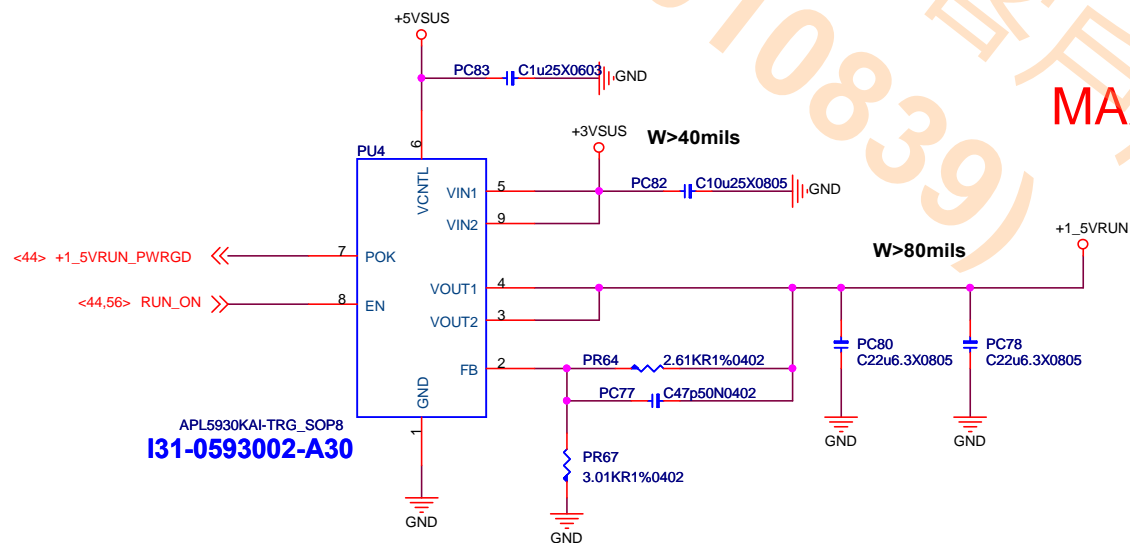


+1.05V RUN

+1_05VRUN / +1_5VRUN

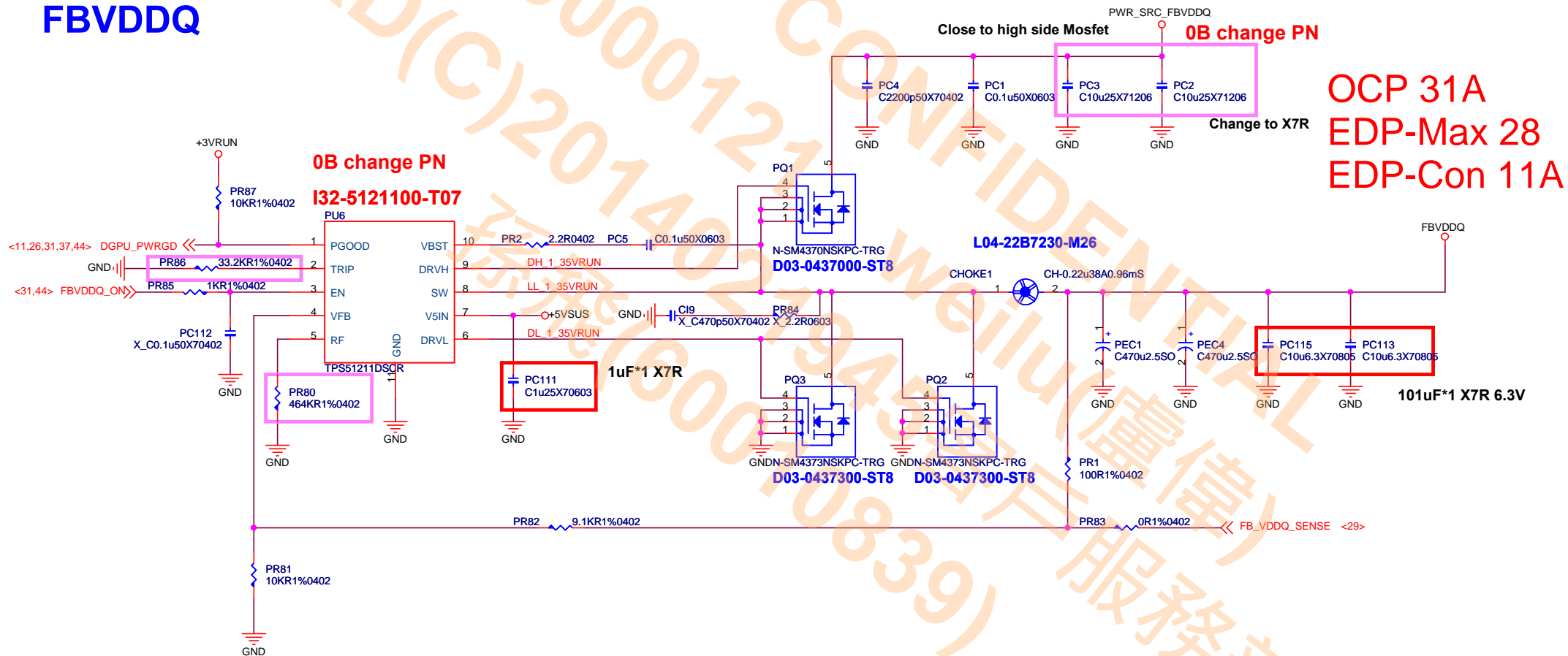


+1.5V RUN



MAX 2A

FBVDDQ

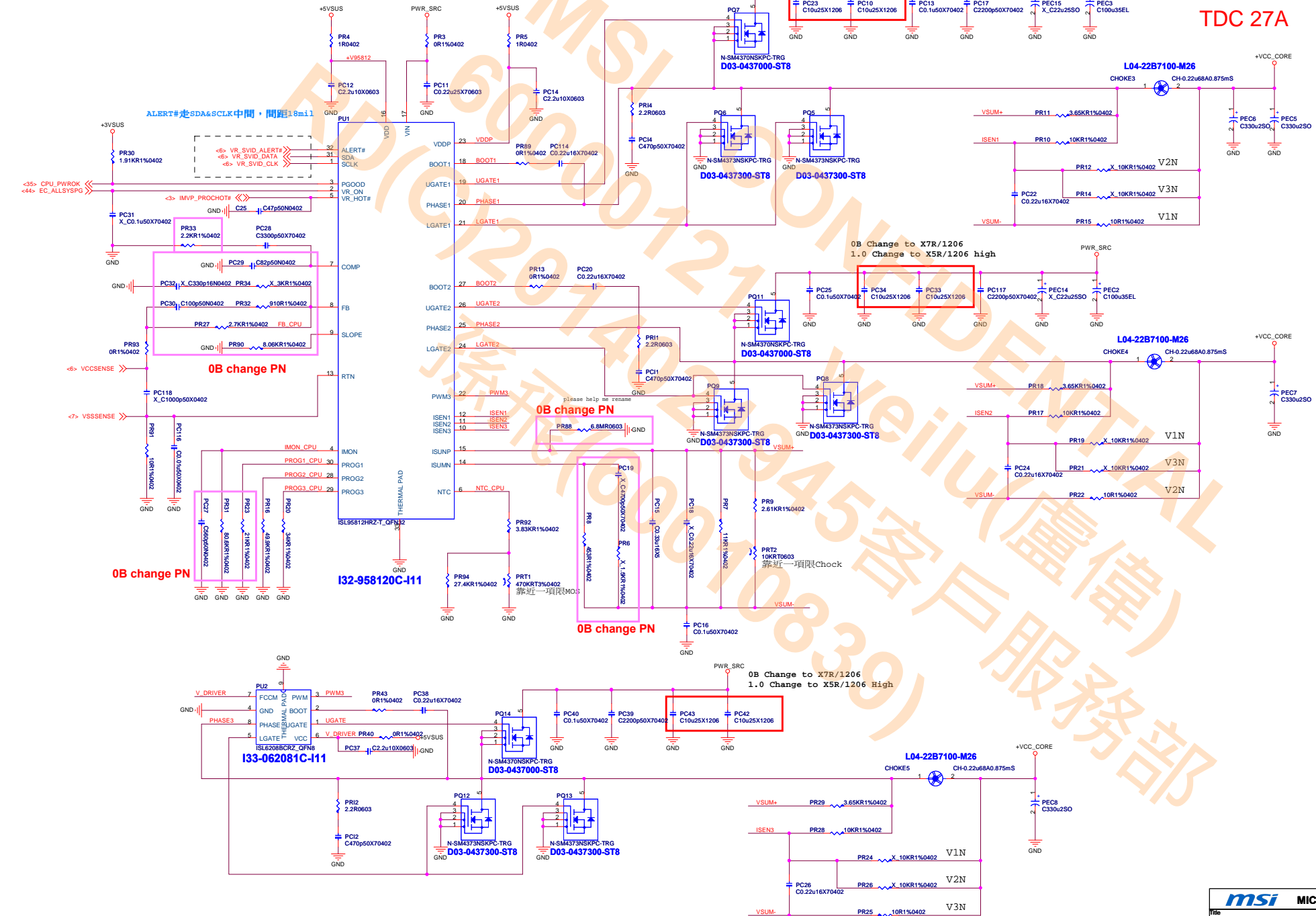


CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

0B Change to X7R/1206
1.0 Change to X5R/1206 high

MAX 95A
TDC 27A



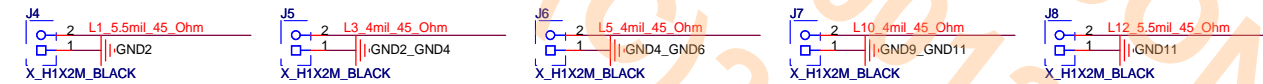
EMI/ Impedance

Impedance Connector No PN

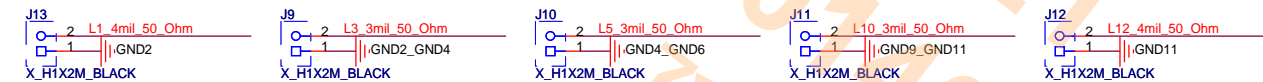
40 ohm



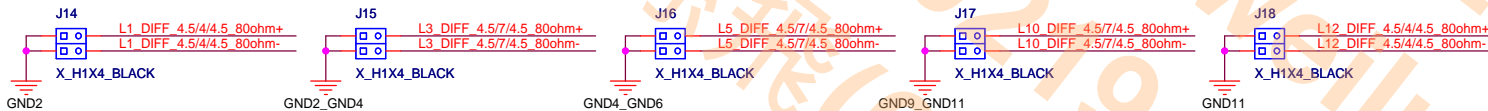
45 ohm



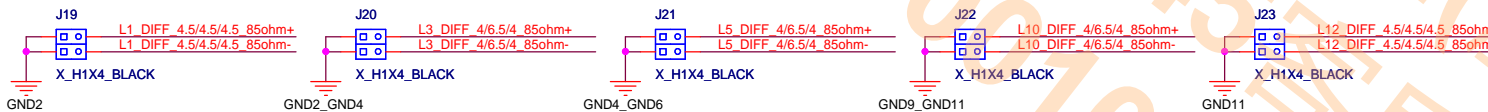
50 ohm



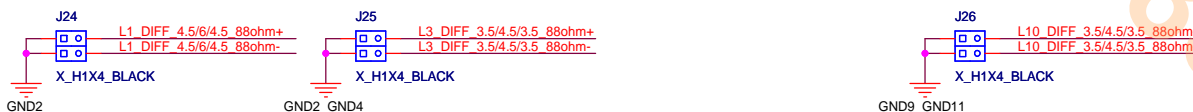
80 ohm



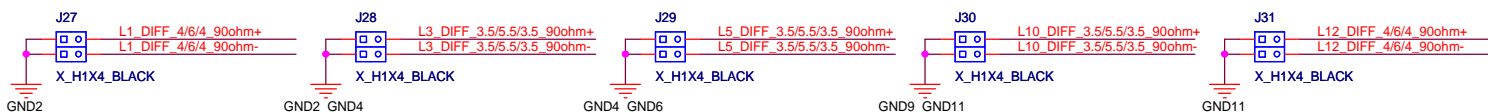
85 ohm



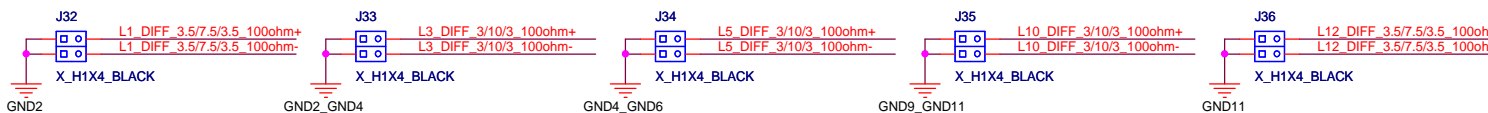
88 ohm



90 ohm

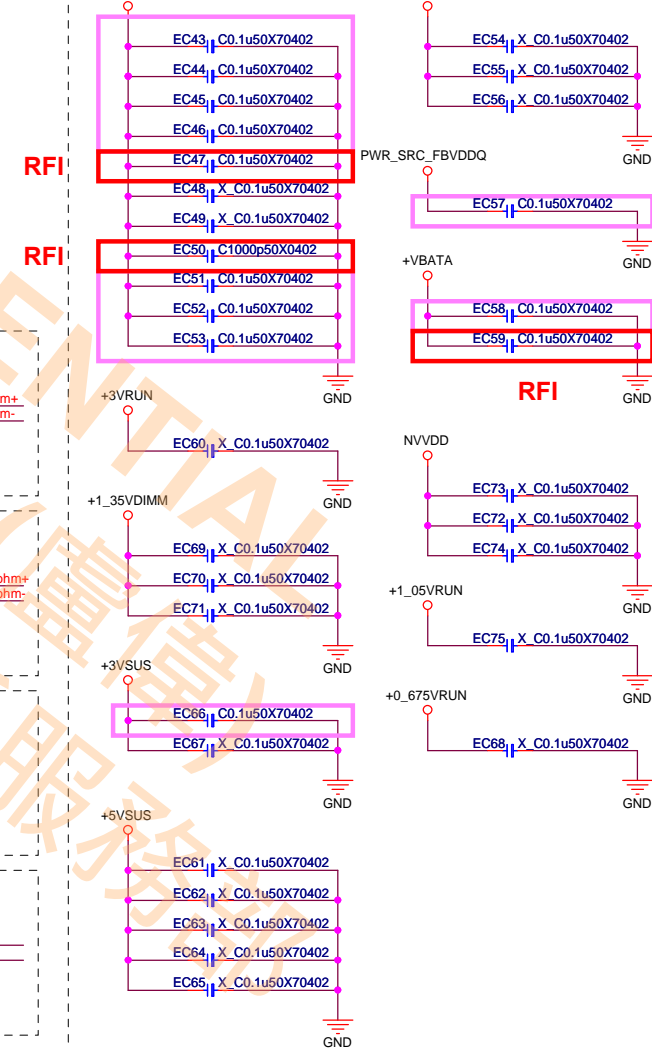


100 ohm



EMI

PWR_SRC 0B stuff

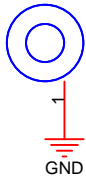


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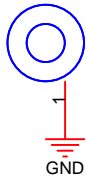
Title			EMI/ Impedance
Size	Document Number	Rev	1.0
MS-16H2			
Date:	Thursday, February 13, 2014	Sheet	62 of 72

CPU/GPU Holes

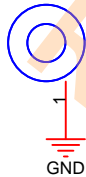
MCPU4 H_R200D150



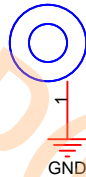
MCPU2 H_R200D150



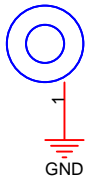
MCPU3 H_R200D150



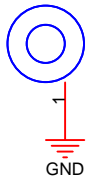
MCPU1 H_R200D150



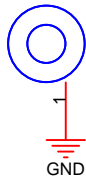
MGPU2 H_R276D169_PB



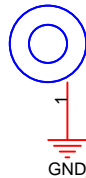
MGPU4 H_R276D169_PB



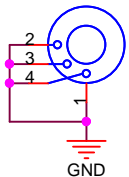
MGPU1 H_R276D169_PB



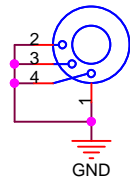
MGPU3 H_R276D169_PB



M2
X_H_R197D118_PT_V3
H_R197D118_PT_V3

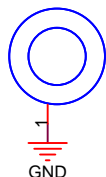


M7
X_H_R197D118_PT_V3
H_R197D118_PT_V3



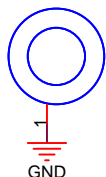
Fan Hole

MH1
H_R197D91
X_ME_ SCREW HOLE

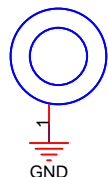


SSD Stand off

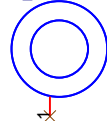
MH3
H_R220D146_PT
E2B-16H2020



MH2
H_R220D146_PT
E2B-16H2020

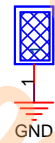


MH4
NPTH157
X_NPTH157



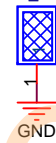
EMI

SPRING1
HS-MS-1721



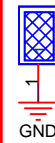
GND
E2M-7213211-CA7
ATE_C006_106

SPRING2
X_HS-MS1011



GND
E23-1011040-CA7
ATE_C006_106

SPRING3
HS-MS-1029



GND
E23-1029060-CA7
ATE_C006_106

MYLAR2

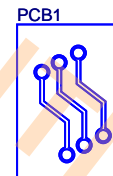
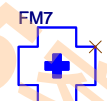
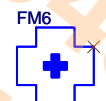
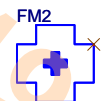
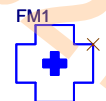
E2M-6H21411-Y42
MYLAR

MYLAR3

E2P-6H22711-Y42
MYLAR

MYLAR4

E2P-6H23011-Y42
MYLAR



PF0-16H2110-H73

PF0-16H2110-H73

Hannstar: PF0-16H2110-H73

TRIPOD: PF0-16H2110-T53

UME1

HDMI
Lable

X_HDMI_ROYALTY

Y01-RHDMI03-000

For MP

UME2

BIOS
Lable

X_BIOS_LABEL

G51-LA01678-A09

RUBBER1

E2Y-6H20711-Y40
RUBBER

RUBBER2

E2Y-6H21311-Y40
RUBBER

RUBBER3

E2Y-6H21311-Y40
RUBBER

BRACKET1

307-6H20111-C22
CPU_BRACKET

BRACKET2

307-6H20111-C22
CPU_BRACKET

BRACKET3

307-6H20211-C22
GPU_BRACKET

MYLAR1

E2P-6H22111-Y42
MYLAR

msi

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Title

Screw/ME

Size

Document Number

MS-16H2

Rev

1.0

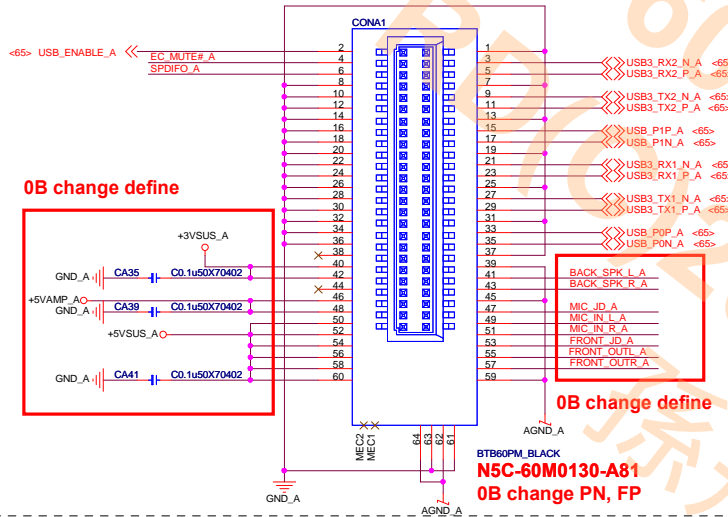
Date: Thursday, February 06, 2014

Sheet 63 of 72

16H2-A Board (Audio CONN)

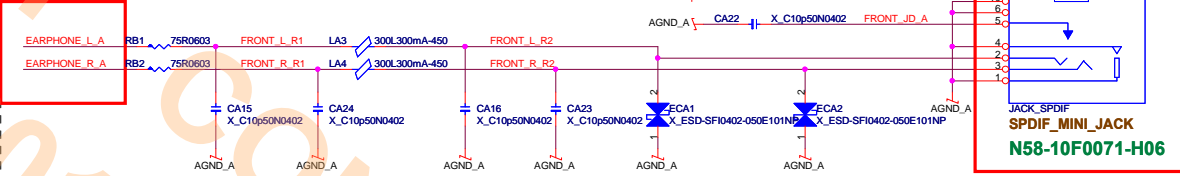
BTB Connector From MB

CONN Pin Current Capability : 0.5A/Pin

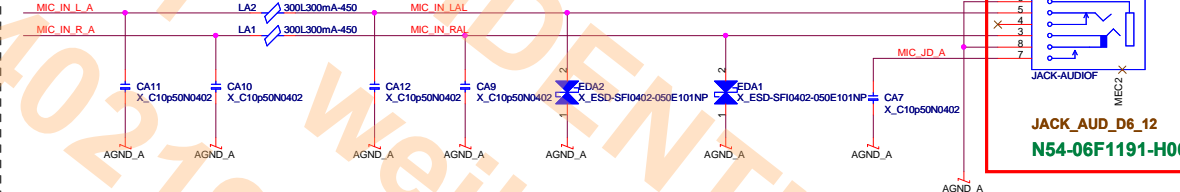


FRONT OUT

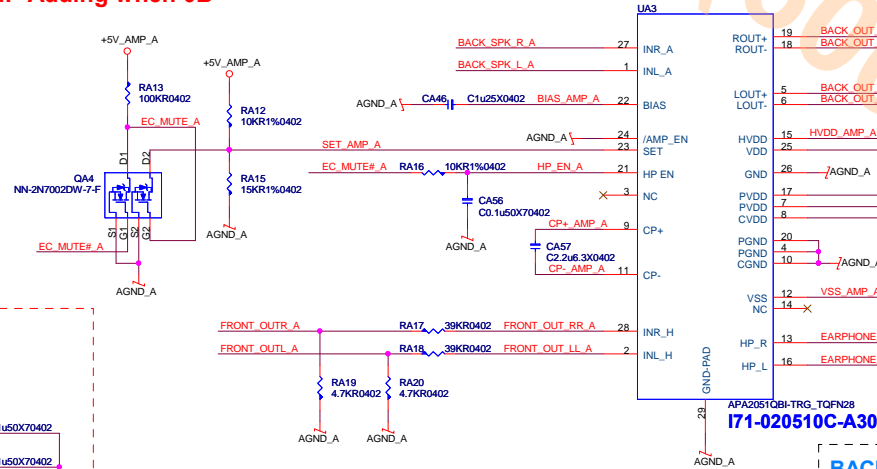
OB change define



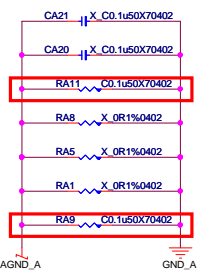
MIC IN



AMP Adding when OB



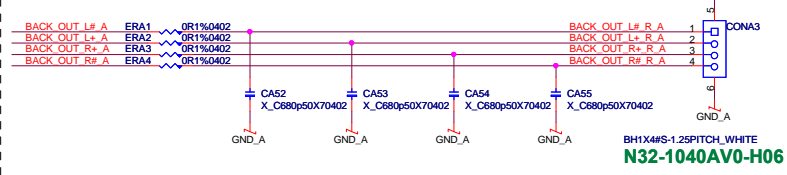
EMI



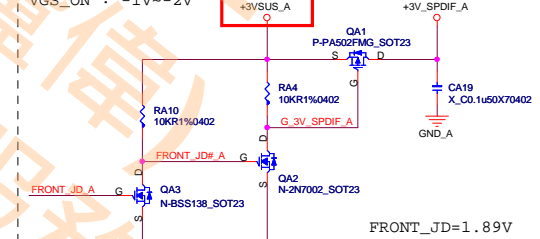
Change to Cap

Change to Cap

BACK SPK CONN

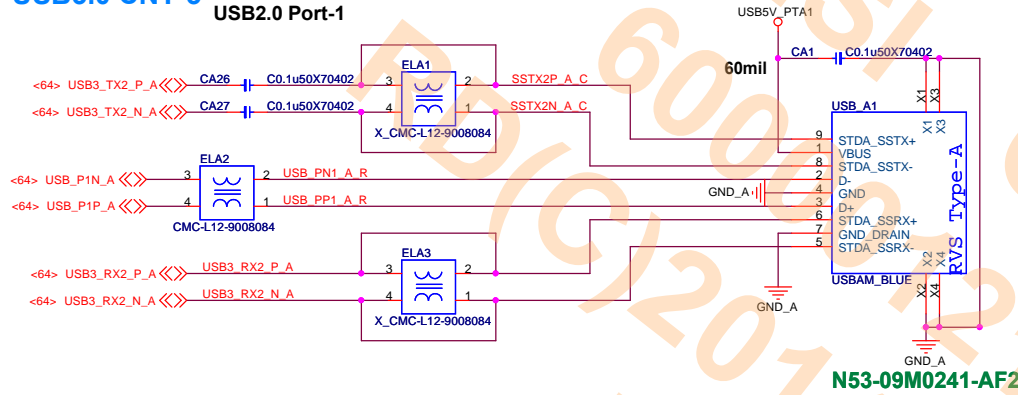


SPDIF Power

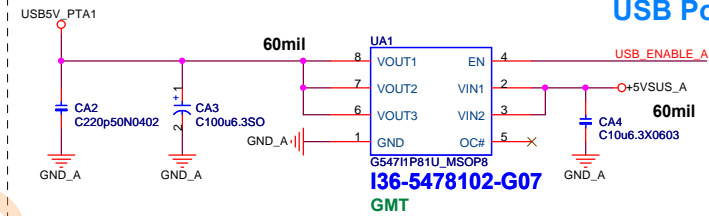


[A] USB3.0 CNT-2/-3

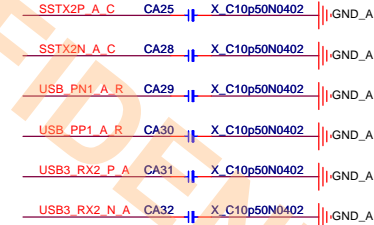
USB3.0 CNT-3 USB3.0 Port-2 USB2.0 Port-1



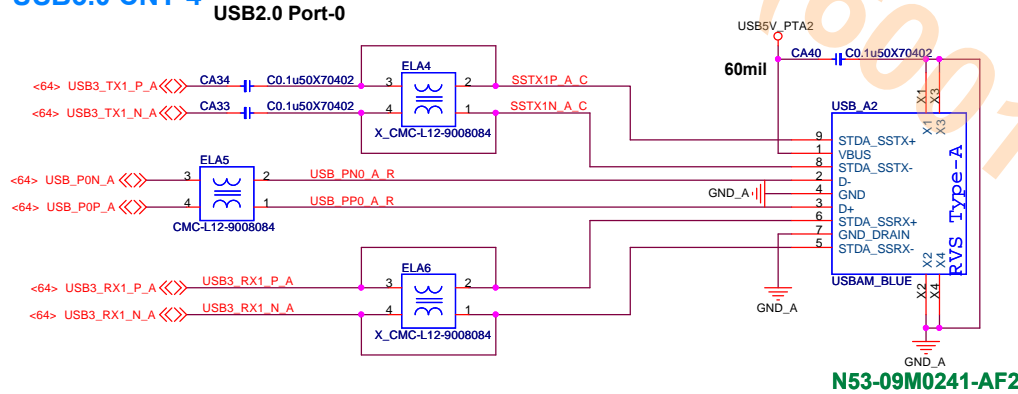
USB Power Switch



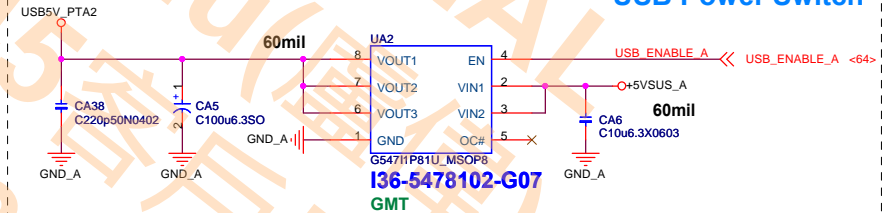
EMI



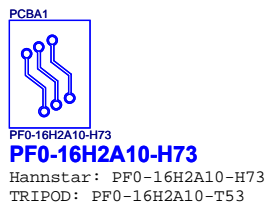
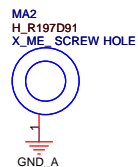
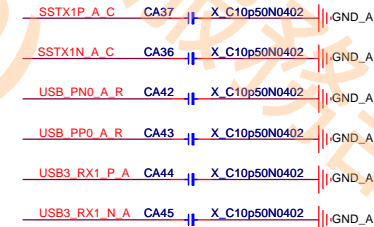
USB3.0 CNT-4 USB3.0 Port-1 USB2.0 Port-0



USB Power Switch



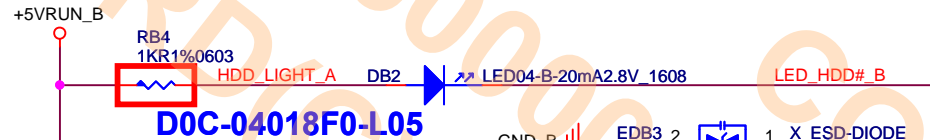
EMI



16H2-B Board (LED Board)

LED

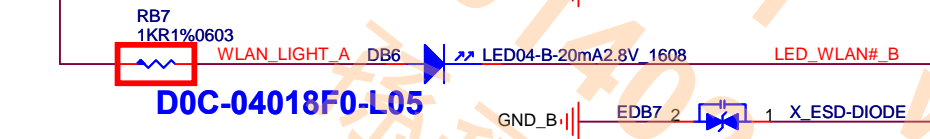
BLUE
(HDD)



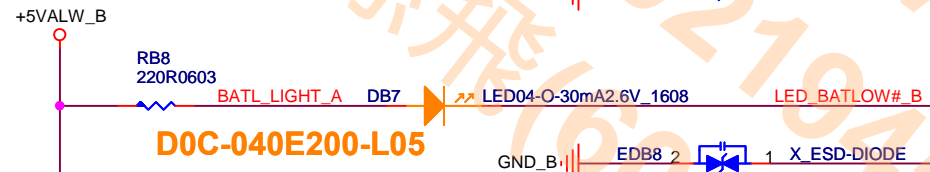
BLUE
(BT)



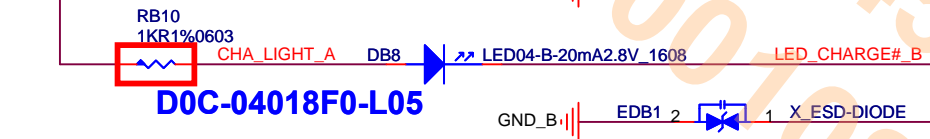
BLUE
(WLAN)



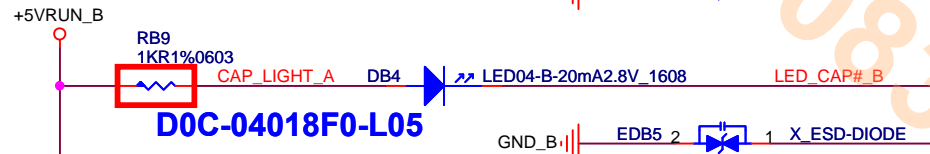
ORANGE
(BATLOW)



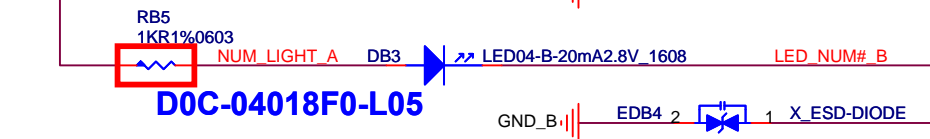
BLUE
(CHARGE)



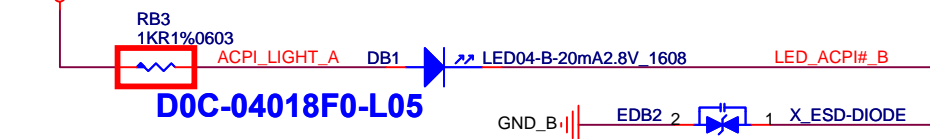
BLUE
(CAP)



BLUE
(NUM)

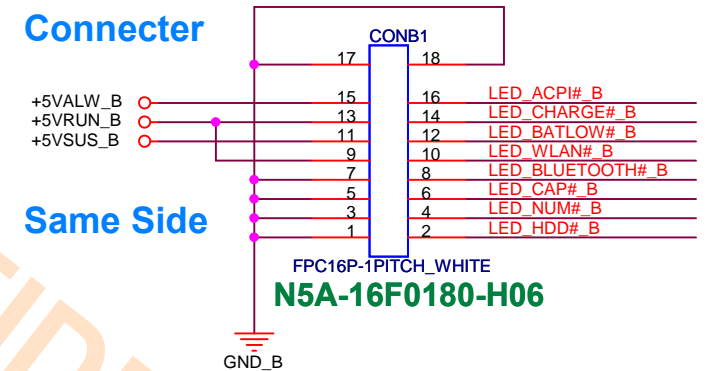


BLUE
(ACPI)

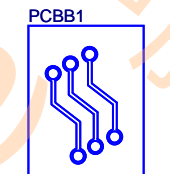


Connector

Same Side

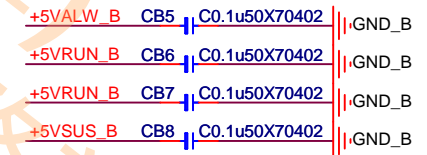
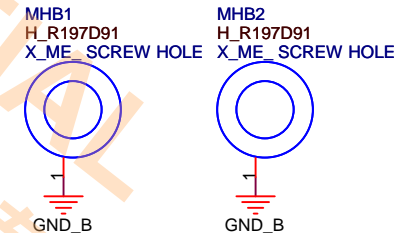


0B add
1.0 Deleted



PF0-16H2B10-H73
PF0-16H2B10-H73

Hannstar: PF0-16H2B10-H73
TRIPOD: PF0-16H2B10-T53



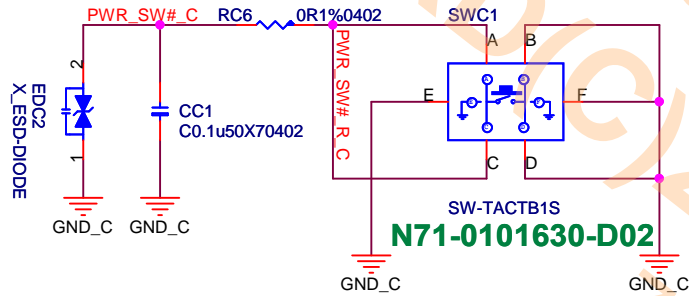
msi

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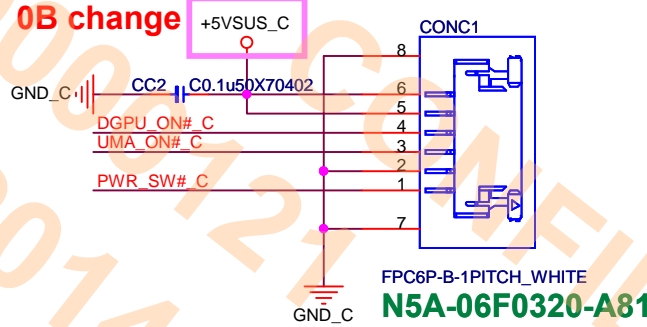
Title			LED Board
Size	Document Number	Rev	
	MS-16H2	1.0	
Date:	Friday, January 03, 2014	Sheet	66 of 72

16H2-C Board (Power SW Board)

Power Switch

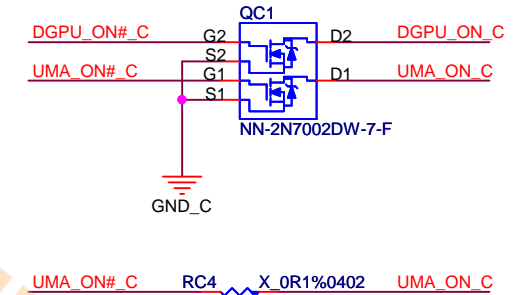


Diff Side Connector



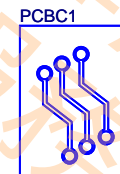
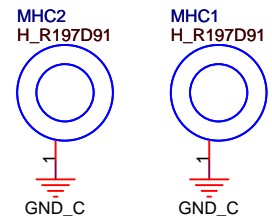
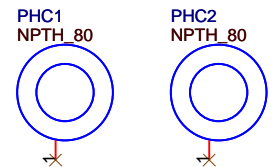
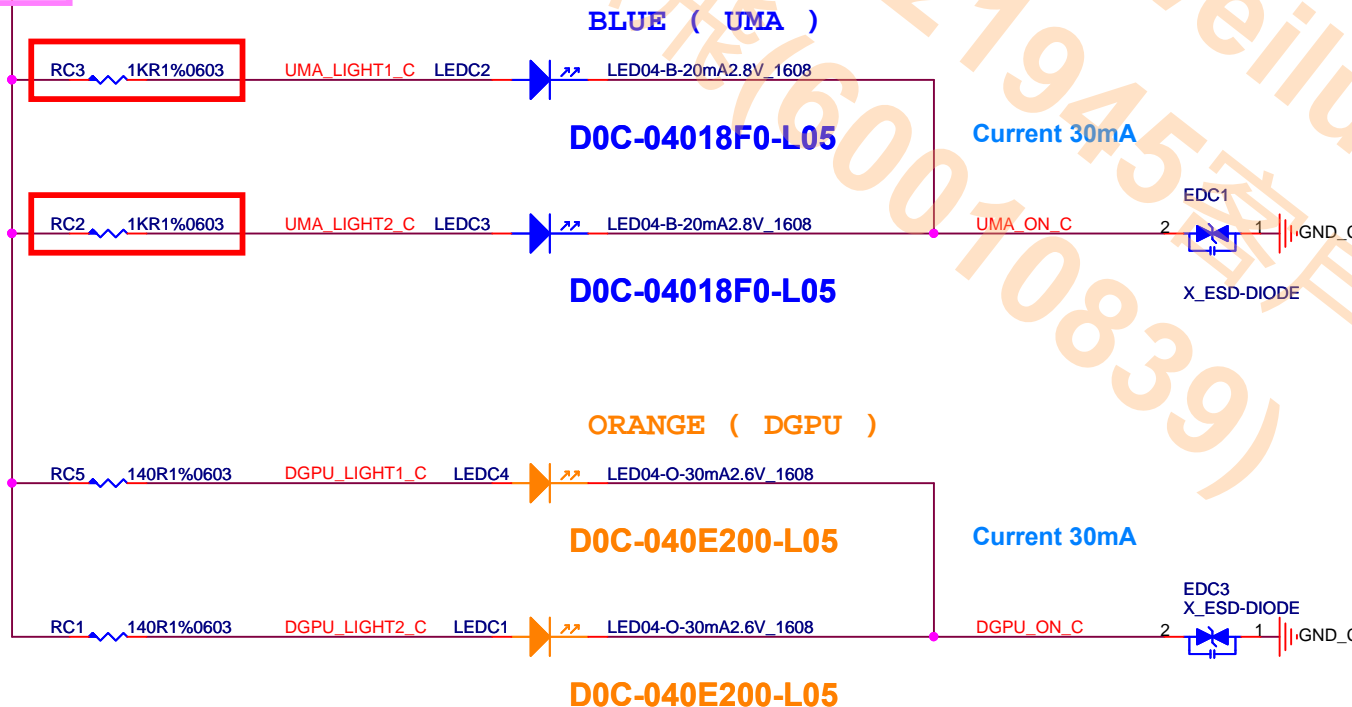
UMA/DGPU Logic

MOS Ton, Toff 20ns



+5VSUS_C 0B change

Power LED



P30-16H2C10-H73
PF0-16H2C10-H73

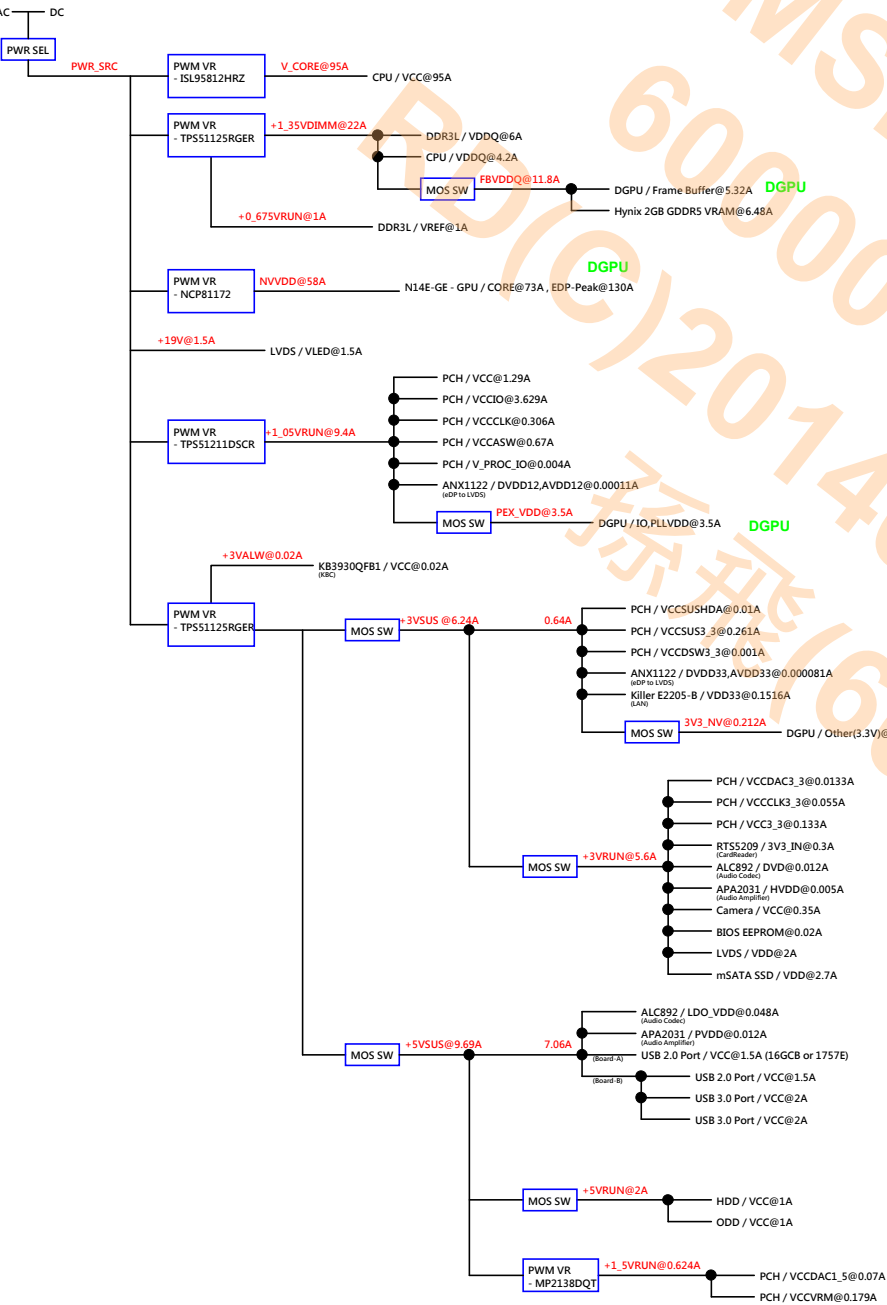
Hannstar: PF0-16H2C10-H73
TRIPOD: PF0-16H2C10-T53

msi

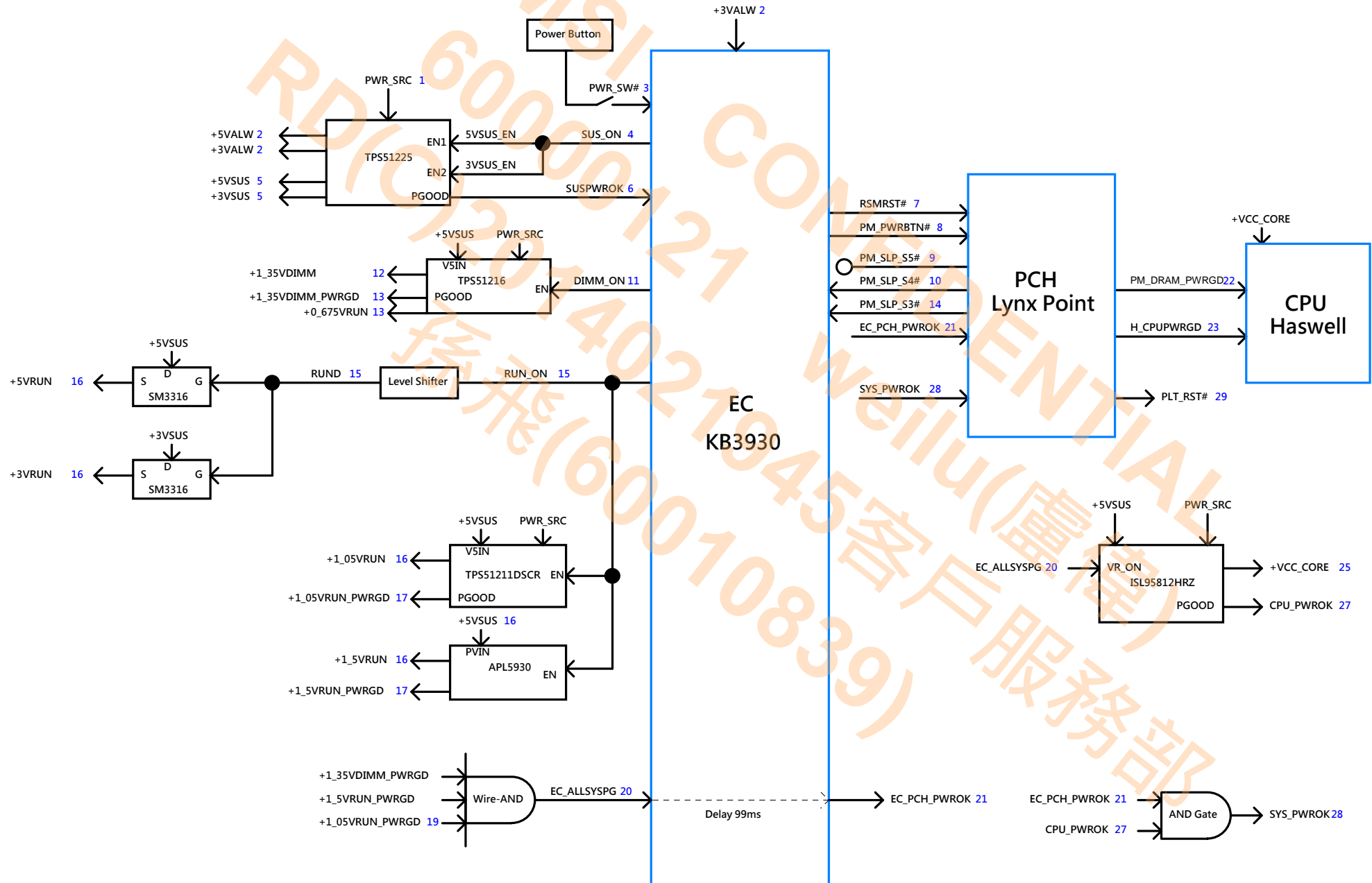
MICRO-STAR INT'L CO.,LTD.

Title			Power SW Board
Size	Document Number	Rev	1.0
Date	Friday, January 03, 2014	Sheet	67 of 72

MS-16H2 Power Delivery Chart

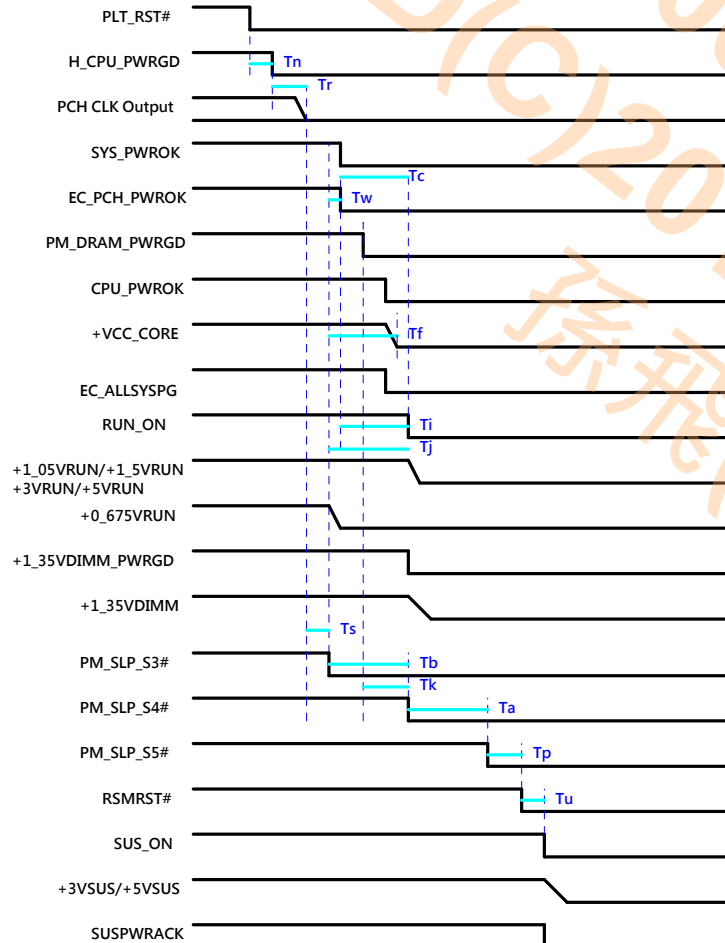


MS-16H2 Power on Block Diagram



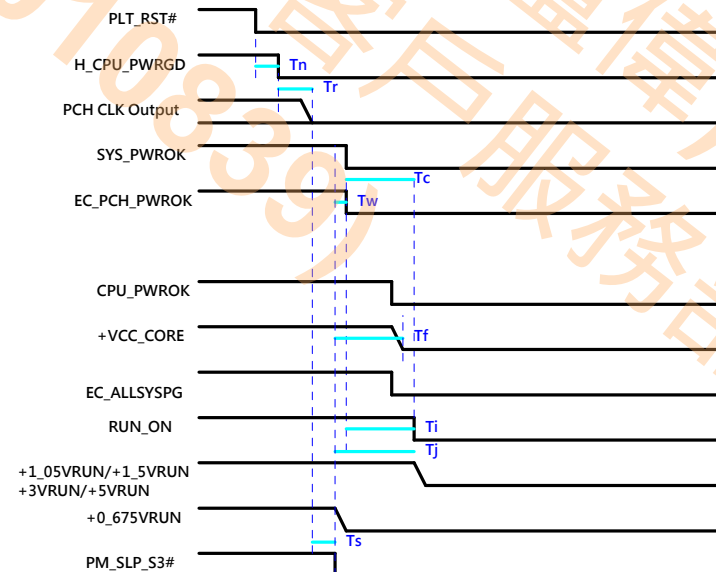
Power down Sequence

S0 -> G3



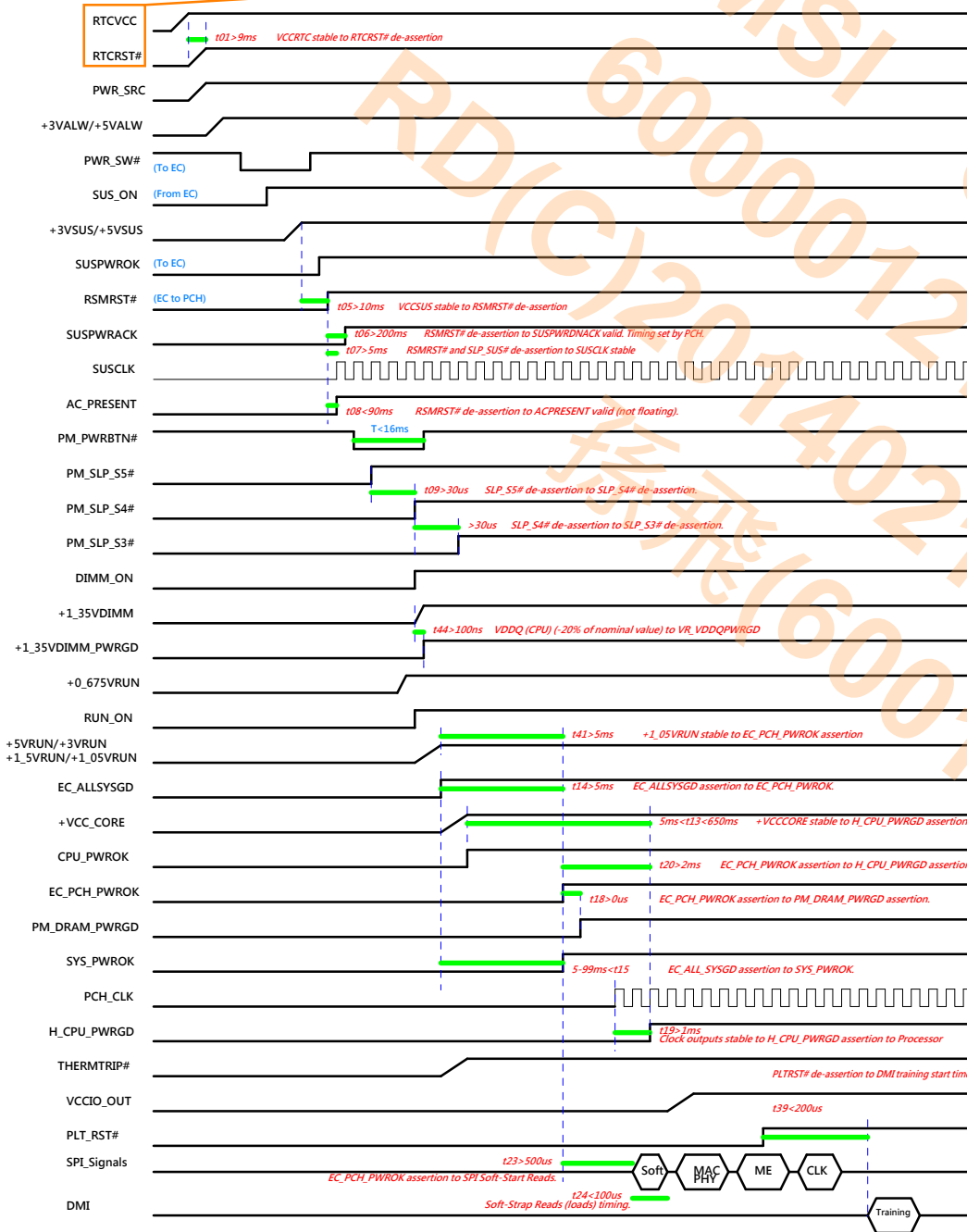
	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3

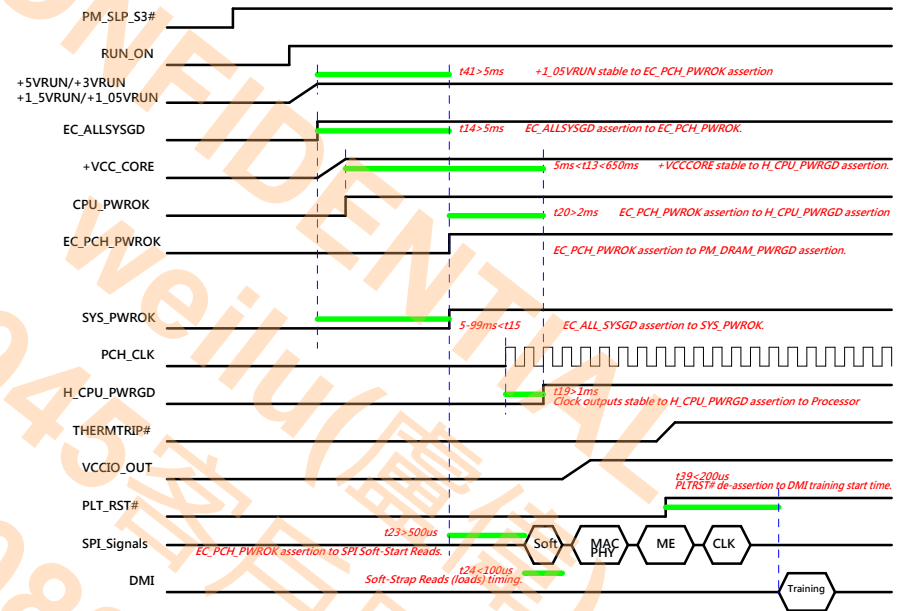


Power on Sequence

G3 -> S0



S3-> S0



History

0B: Hardware part

- 01. Remove All GAP for power parts.
- 02. Add 3V3_NV part for leakage
- 03. Change cardreader PN.
- 04. Change BTB PN
- 05. Change SPDIF/ Audio Jack PN
- 06. R116 unstuff, R117 stuff.
- 07. R346 unstuff
- 08. Remove SUBWOOFER
- 09. Add one more AMP for SPK

0B: Power part

- 01. PR33 2.2Kohm R11-0222T12-W08
- 02. PC29 82pF/50V C11-8201012-W08
- 03. PC30 100pF/16V C11-1011032-W08
- 04. PR34 unstuff
- 05. PC32 unstuff
- 06. PR27 2.7Kohm R11-0272T12-W08
- 07. PR90 8.06Kohm R11-8061T12-W08
- 08. PR32 910Rohm R11-0911T12-W08
- 09. PC27 560pF/16V C11-5611812-W08
- 10. PR31 80.6Kohm R11-8062T12-W08
- 11. PR23 21Kohm R11-0213T12-W08
- 12. PR88 6.8Mohm R11-0685T13-W08
- 13. PR8 453Rohm R11-4530T22-W08
- 14. PC19 unstuff
- 15. PR6 unstuff
- 16. PR140 100Kohm R11-0104T12-W08
- 17. PR145 93.1Kohm R11-9312T12-R01
- 18. PR143 15Kohm R11-0153T12-W08
- 19. PR124 95.3Kohm R11-9532T12-W08
- 20. PR86 28.7Kohm R11-2872T12-W08
- 21. PC69, PC70 change to 1206 package
- 22. PR88 6.8Mohm R11-0685T13-W08